Venkatesh Akella

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Department of Electrical & Computer Engineering
University of California
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EDUCATION

University of Utah, Salt Lake City, UTAH — 1992
Ph.D. in Computer Science

Indian Institute of Science, Bangalore, India — 1988
M.S. in Electrical & Computer Engineering

Andhra University, Waltair, India — 1986
Bachelors in Engineering Electronics & Communication Engineering

AWARDS AND HONORS

- Best Paper Nomination, ACM International Conference on Embedded Software (EMSOFT), 2009.
- National Science Foundation CAREER Award 1997
- President's Fellowship, University of Utah, 1989 –1991
- Gold Medal for University-wide First Rank, Andhra University, 1986

ACADEMIC EXPERIENCE

2017-2018, Faculty Director Online Graduate Programs, University of California, Davis

2010-2012, Chair, ECE Graduate Program and Vice Chair Department of Electrical & Computer Engineering, University of California, Davis

2009-2010: ABET Coordinator, Department of Electrical & Computer Engineering, University of California, Davis.

2006 - Present: Professor of Electrical and Computer Engineering, University of California, Davis

1998-2006: Associate Professor of Electrical and Computer Engineering, University of California, Davis

1992-1998: Assistant Professor of Electrical and Computer Engineering, University of California, Davis

INDUSTRY EXPERIENCE

Visiting Professor Indian Institute of Management, Bangalore, 1999
Research in Valuation of Intellectual Property and Design Reuse and Off-shore Software Development

Visiting Professor, Hewlett-Packard, Roseville, CA - 1996
Developed a methodology for the verification of complex application-specific integrated circuits used in fiber channel products

Director of Engineering, eXtensil Inc, Sunnyvale, CA, 2000-2002
Member of founding team; Defined the product architecture of a high-performance and low-power reconfigurable logic based platform for wireless communication; Architect of the EDA tool chain; managed the development of EDA software in India and Australia; Member of Technical Advisory Board

Technical Consultant, Silicon Automation Systems, Sunnyvale, CA, 1998-2000
Developed a hardware/software codesign methodology for Sharp's data-driven media processor (asynchronous processor for media processing); Defined and supervised the implementation of the complete codesign tool chain; Developed Plans for a Design Center

Founder and Vice President (Products), Concesta Inc, San Mateo, CA, 2005-2007
Electronic Commerce business, developed business plans, marketing and fundraising

Technical Consultant, DSM Solutions, Los Gatos, CA, 2007-2009
Technology Evaluation, Technical Marketing and Product Definition

RESEARCH FUNDING

1. DoD/National Security Agency - Ultra-Low Latency Low-Power All-Optical Interconnection switch for Petascale Computing (PI- Yoo, Co-PI Akella) $657742, 8/2009 – 9/2012
2. National Science Foundation (NSF) – Improving Trace-based Simulation of On-Chip Networks (PI- Akella, Co-PI Farrens), $448,835, 7/2011 – 6/2014
3. Department of Education – GAANN: Resilient Information Systems Targeting Societal-Scale Applications (PI's Akella, Chuah, Levy) $760,000, 8/2006 to 8/2009
4. Intel Research– Leveraging WDM-based Optical CPU-DRAM Interconnects for Data Mining Workloads - (PI –Akella) – $50,000 Unrestricted gift
5. Nokia Research – Repurposing Cell Phones for Surveillance Applications ($9000, unrestricted gift, Co-PI Prof. Amiratharajah and Prof. Fred Chong, UCSB)

6. Intel Research– Wireless Multimedia Algorithms and Architectures - (PI – Prof. van der Schaar, Co-PI Akella) – $120,000
7. Intel Research – Network Processors for Wireless Multimedia ($20000, unrestricted gift)
8. National Science Foundation (NSF) Dynamic Resource Management for Multimedia Applications on Embedded Systems(PI: Prof. van der schaar, UCLA and Co-PI Akella) – $270,000, September 1, 2005-August 30, 2008.
9. National Science Foundation (NSF) – Programmable Architectures for Low Density Parity Check Codes - (PI: Akella and Co-PI Shu Lin) – $150,000, September 1, 2004-August 30, 2007.
10. National Science Foundation (NSF) – Programmable Language and Middleware Support for Sensor Network Applications - (PI Prof. Pandey and Co-PI: Prof. Akella) $617,954, September 1, 2004 – August 31, 2007
11. National Science Foundation (NSF) – NeTS-NR – High Performance Networking Technology and Systems For Heterogeneous Networks, (PI – Prof. Yoo, Co-PI – Akella and Levitt) - $305,000 – October 1, 2004 – September 30, 2006.
12. National Science Foundation (NSF) - ITR: SynchroScalar: A Tile-based Embedded Processor for Energy Efficient Multirate Embedded Systems (PI – Akella & Chong and Co-PI Prof. Baas) - $300,000 - 08/15/03 to 7/31/06
13. National Science Foundation (NSF) - Unified Networking Research Testbed for the Next Generation Optical Internet (PI – Yoo and co-PI – Akella, Chuah and Heritage) $300,000 - 10/01/03. to 9/30/05
14. Analog Devices, MA – Integration of DSP with Reconfigurable Logic - (Unrestricted gift) (PI – Akella) $22,500.
15. National Science Foundation (NSF) – Making Asynchronous Design Practical – CAREER Award; $202,456, 1997 – 2001(PI – Akella)
16. University of California, Faculty Research Award – Low Power Design Using Clock Gating, $3000 ; 1997-1998
17. National Security Agency (NSA) - Compositional Framework for Supporting Design Evolution of Secure Systems (PI – Akella Co-PI: Prof. Levitt) - $97,143, 1996-1997
18. National Science Foundation (NSF) – High-level Synthesis of Self-timed Circuits, $100,000 – 1993-1996 (PI – Akella)
19. University of California, Faculty Research Award – Asynchronous Design, $5000, 1993-1994

GRADUATE STUDENTS (CURRENT)

	Name	**Deg**	**Topic**
1	Huan Zhang	Ph.D.	Large Scale Machine Learning – Algorithms and Implementation
2	Kramer Straube	Ph.D.	Constant Average Power Processing for Heterogeneous Computing Platforms
3	Terry O'Neill	Ph.D.	Deep Learning in Agriculture
4.	Jennifer Priscilla	M.S.	Galois Field Fourier Transforms on a FPGA

GRADUATE STUDENTS (PAST)

	Name	Deg	Year	Topic	Last Known Coordinates
1	Robert St. Denis	MS	2017	Asynchronous Caches	
2	Sandeep Rasoori	MS	2017	Accelerating Stochastic Gradient Descent on a FPGA	Intel, Folsom
3	Sree Balaji Girishankar	MS	2017	FPGA Implementation of Iterative Soft Decision Decoder for (127,119) Reed Solomon Codes	Intel, San Jose
4	Christine Saundry	MS	2015	Cache Design for Near-threshold Processors	Lockheed Martin
5	Frank Maker (co-advisor R. Amirtharajah)	PhD	2013	CPU-GPU Codesign	Roku Systems
6	Christopher J Nitta (co-advisor Matt Farrens)	PhD	2011	Optical Interconnects for Energy Efficient Computer Systems	Adjunct Assistant Professor UC Davis
7	Kevin MacDonald	MS	2011	Techniques for Inferring Packet Dependencies to Improve Trace-Based Simulation of On-Chip Networks	Synopsys
8	Xiaoheng Chen	PhD	2011	Reconfigurable Computing for High Performance Signal Processing	Microsoft
9	John Oliver	PhD	2007	Synchronoscalar: Low Power Multicore Architecture for Embedded Processing	Assistant Professor, Calfornia State University, San Luis Obispo (CalPoly)
10	Haijun Yan (Co-advisor S. J. Ben Yoo)	PhD	2007	Architecture and Scheduling Algorithms for an All Optical Core Router	Cisco Systems, San Jose
11	Ravi shankar Rao	PhD	2006	Modeling and Microarchitecture for low power	SMachines, Folsom (startup)
12	Julie Taylor	MS	2003	Edge Routers and Active Queue Management	Lockheed Martin, Sunnyvale, CA
13	Yash Bansal	MS	2002	Optical Core Router	Network Sound, CA
14	Gregory Valdez	MS	2001	Cosimulation and Dynamic Reconfiguration	Sandia National Laboratories,

					Livermore, CA
15	Michael Foster	MS	2000	Hardware/Software Codesign from Simulink	Agilent Technologies, Santa Rose, CA
16	Tony Werner	PhD	2000	Asynchronous Superscalar Processor	Cisco Systems, CA
17	Robert J. Gluss	MS	1999	Radix-4 Asynchronous Floating Point Divider	Intel, Santa Clara, CA
18	Nithya Raghavan	MS	1997	Low Power Clock Gating	Cisco
19	Carrie Artang	MS	2000	Performance Driven Clock Gating from RTL Descriptions	Intel, Folsom
20	Navjot Birak	MS	1995	Self-timed CMOS Cell Library	Hewlett Packard, Roseville, CA
21	David Johnson	MS	1996	Micropipelined Discrete Cosine Transform Processor	IDAX Systems, Virginia
22	Bret Stott	MS	1995	Asynchronous DCT Processor	Rambus Cupertino
23	Kapilan Maheswar	MS	1995	Self-timed FPGA	Lucent
24	J. Lipsher	MS	1994	Asynchronous Design	Grass Valley Group

RESEARCH PAPERS PUBLISHED

1. G. Gopalakrishnan, N. Mani, and V. Akella. PARALLEL COMPOSITION OF LOCKSTEP SYNCHRONOUS PROCESSES FOR HARDWARE VALIDATION: DIVIDE-AND-CONQUER COMPOSITION. Proceedings of the Workshop on Automatic Verification Methods for Finite State Systems, pp. 375-382. 1989

2. G. Gopalakrishnan, R. Fujimoto, V. Akella, N. Mani, and K. Smith. SPECIFICATION-DRIVEN DESIGN OF CUSTOM HARDWARE IN HOP. Current Trends in Hardware Verification and Automated Theorem Proving, edited by Birtwistle and Subrahmanyam, Chapter 3, pp. 128-170. 1989

3. G. Gopalakrishnan, R. Fujimoto, and V. Akella. HOP: A PROCESS MODEL FOR SYNCHRONOUS HARDWARE; SEMANTICS AND EXPERIMENTS IN PROCESS COMPOSITION. Integration, the VLSI Journal, Vol. 8, pp. 209-247. 1989

4. G. Gopalakrishnan, N. Mani, and V. Akella. A DESIGN VALIDATION SYSTEM FOR SYNCHRONOUS HARDWARE BASED ON A PROCESS MODEL: A CASE STUDY. Proceedings of the IMEC-IFIP International Workshop on Formal VLSI Specification and Synthesis VLSI Design Method-I, pp. 227-247. 1989

5. G. Gopalakrishnan, P. Jain, V. Akella, L. Josephson, and W -Y Kuo. COMBINING VERIFICATION AND SIMULATION. Proceedings of the 1991 UC Santa Cruz Conference on Advanced Research in VLSI, pp. 323-339,1991

6. Venkatesh Akella and G. Gopalakrishnan. HIGH LEVEL TEST GENERATION VIA PROCESS COMPOSITION. Designing Correct Circuits, edited by Geraint Jones and Mary Sheeran. Springer-Verlag (London) ISBN 3-540-19659-5, pp. 99-119. 1991

7. Venkatesh Akella and G. Gopalakrishnan. HIERARCHICAL ACTION REFINEMENT: A METHODOLOGY FOR COMPILING ASYNCHRONOUS CIRCUITS FROM A CONCURRENT HDL. Proceedings of the Tenth International Symposium on Computer Hardware Description Languages and their Applications, CHDL-91, pp. 351-369. 1991

8. Venkatesh Akella and G. Gopalakrishnan. FROM PROCESS-ORIENTED FUNCTIONAL SPECIFICATIONS TO EFFICIENT ASYNCHRONOUS CIRCUITS. Proceedings of the Fifth International Conference on VLSI. 1992

9. Venkatesh Akella and G. Gopalakrishnan. FLOW ANALYSIS TECHNIQUES FOR THE SYNTHESIS OF EFFICIENT ASYNCHRONOUS CIRCUITS. Proceedings of the Second ACM/SIGDA Workshop on Timing Issues in the Specification and Synthesis of Digital Systems, 13 pages. 1992

10. V. Akella and G. Gopalakrishnan. SHILPA: A HIGH-LEVEL SYNTHESIS SYSTEM FOR SELF-TIMED CIRCUITS. Proceedings of the International Conference on Computer Aided Design (ICCAD), pp. 587-591. 1992

11. G. Gopalakrishnan and V. Akella. VLSI ASYNCHRONOUS SYSTEMS: SPECIFICATION AND SYNTHESIS. Microprocessors & Microsystems, Vol. 16, No. 10, pp. 517-527. 1992

12. J-L. Sung and V. Akella. IMPLEMENTING DELAY INSENSITIVE SELF-TIMED CIRCUITS WITH SINGLE-RAIL DATA SIGNALS. ACM International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems, 11 pages. 1993

13. G. Gopalakrishnan and V. Akella. SPECIFICATION, SIMULATION, AND SYNTHESIS OF SELF-TIMED CIRCUITS. Proceedings of the 26th Annual Hawaii International Conference on System Sciences, Vol. I, pp. 399-408. 1993

14. G. Gopalakrishnan and V. Akella. A TRANSFORMATIONAL APPROACH TO ASYNCHRONOUS HIGH-LEVEL SYNTHESIS. Proceedings of the International Conference on Very Large Scale Integration (VLSI 93) 1993

15. V. Akella and G. Gopalakrishnan. CFSIM: A CONCURRENT COMPILED- CODE FUNCTIONAL SIMULATOR FOR hopCP. International Journal in Computer Simulation, Vol. 4, No. 4, pp. 375-393, 1993

16. V. Akella and G. Gopalakrishnan. SPECIFICATION AND VALIDATION OF CONTROL-INTENSIVE IC'S IN hopCP. IEEE Transactions on Software Engineering, Vol. 20, No. 6, pp. 405-423,1994

17. G. Gopalakrishnan and V. Akella. HIGH-LEVEL OPTIMIZATIONS IN COMPILING PROCESS DESCRIPTIONS TO ASYNCHRONOUS CIRCUITS. Journal of VLSI Signal Processing, Vol. 7, pp. 33-45., 1994

18. P. Kudva and V. Akella. TESTING TWO PHASE TRANSITION SIGNALING BASED SELF-TIMED CIRCUITS IN A SYNTHESIS ENVIRONMENT. Proceedings of the Seventh International Symposium on High-Level Synthesis, pp. 103-111. 1994

19. P. Kudva, G. Gopalakrishnan, and V. Akella. PERFORMANCE ANALYSIS OF ASYNCHRONOUS CIRCUITS USING TIMED PETRI NETS. International Conference on Computer Design (ICCD-94), pp. 166-175 1994

20. P. Kudva and V. Akella. A TECHNIQUE FOR ESTIMATING POWER IN ASYNCHRONOUS CIRCUITS. First International Symposium on Asynchronous Circuits and Systems, pp. 166-175. 1994

21. P. Reddy and V. Akella. DESIGN OF AN ADAPTIVE SMART CARD WITH IN-LAB EXPERIMENTS. Proceedings of the IEEE-IEE Vehicle Navigation and Information Systems Conference, 6 pages. 1995

22. P. Kudva, G. Gopalakrishnan, and V. Akella. HIGH LEVEL SYNTHESIS OF ASYNCHRONOUS CIRCUIT TARGETING STATE MACHINE CONTROLLERS. International Conference on Hardware Description Languages (CHDL 95), pp. 605-610. 1995

23. B. Stott, D. Johnson, and V. Akella. ASYNCHRONOUS 2-D DISCRETE COSINE TRANSFORM CORE PROCESSOR. Proceedings of the International Conference on Computer Design (ICCD-95). 1995

24. T. Werner, V. Akella. COUNTERFLOW PIPELINE BASED DYNAMIC INSTRUCTION SCHEDULING. Proceedings of Second International Symposium on Advanced Research in Asynchronous Circuits and Systems, pp. 69-79. 1996

25. V. Akella, N. Vaidya, R. Redinbo. LIMITATIONS OF VLSI IMPLEMENTATION OF DELAY-INSENSITIVE CODES. Proceedings of Annual Symposium on Fault Tolerant Computing, pp. 208-217. 1996

26. T. Werner and V. Akella. ASYNCHRONOUS PROCESSOR SURVEY. IEEE Computer, Vol. 30, No. 11, pp. 67-76. 1997

27. K. Maheswar and V. Akella,. PGA-STC: A PROGRAMMABLE GATE ARRAY FOR SELF-TIMED CIRCUITS. International Journal of Electronics, Vol. 84, No. 3, pp. 255-267. 1998

28. D. Johnson and V. Akella. DESIGN AND ANALYSIS OF ASYNCHRONOUS ADDER. IEE Proceedings for Computers and Digital Techniques, Vol. 145, No. 1, pp. 1-8. 1998

29. D. Johnson, V. Akella, and B. Stott. MICROPIPELINED SYNCHRONOUS DISCRETE COSINE TRANSFORM (DCT/IDCT) PROCESSOR. IEEE Transactions on VLSI Systems, Vol. 6, No. 4, pp. 731-740. 1998

30. V. Akella, N. H. Vaidya, and G. R. Redinbo. ASYNCHRONOUS COMPARISON-BASED DECODERS FOR DELAY-INSENSITIVE CODES. IEEE Transaction on Computers, Vol. 47, No. 7, pp. 802-811. 1998

31. R. Pandey, V. Akella, and P. Devanbu. SUPPORT FOR EVOLUTION OF THE SYSTEMS THROUGH SOFTWARE COMPOSITION. Proceedings of the International Workshop on the Principles of Software Evolution, pp. 1-6, 1998

32. N. Raghavan, V. Akella, and S. Bakshi. AUTOMATION INSERTION OF GATED CLOCKS AT REGISTER TRANSFER LEVEL. Proceedings of the Twelfth International Conference on VLSI Design, IEEE Computer Society, pp. 48-54. 1999

33. T. Werner and V. Akella. AN ASYNCHRONOUS SUPERSCALAR ARCHITECTURE FOR EXPLOITING INSTRUCTION-LEVEL PARALLEISM. Proceedings of the International Symposium on Advanced Research on Asynchronous Circuits and Systems, ASYNC 2001, March, pp. 140-151.

34. S.J.B. Yoo, Y. Bansal, Z. Pan, J. Cao, V.K. Tsui, S.K.H. Fong, Y. Zhang, J. Taylor, H.J. Lee, M. Jeon, and V. Akella. OPTICAL-LABEL BASED PACKET ROUTING SYSTEM WITH CONTENTION RESOLUTION IN WAVELENGTH, TIME, AND SPACE DOMAINS. In Optical Fiber Conference, OFC, 2002

35. Z. Pan, J. Cao, Y. Bansal, V.K. Tsui, S.K.H. Fong, Y. Zhang, J. Taylor, H.J. Lee, M. Jeon, V. Akella, S.J.B. Yoo, K. Okamoto, and S. Kamei. ALL-OPTICAL PROGRAMMABLE TIME-SLOT-INTERCHANGER USING OPTICAL-LABEL SWITCHING WITH TUNABLE WAVELENGTH CONVERSION AND N AND N ARRAYED WAVEGUIDE GRATING ROUTERS. In Optical Fiber Conference, OFC, 3 pg. 2002

36. Z. Pan, M. Y. Jeon, Y. Bansal, J. Cao, J. Taylor, V. Akella, S. Kamei, K. Okamoto, and S. J. B. Yoo. PACKET-BY-PACKET WAVELENGTH, TIME, SPACE-DOMAIN CONTENTION RESOLUTION IN AN OPTICAL-LABEL SWITCHING ROUTER WITH 2R REGENERA-TION. IEEE Photonics Technology Letters, Vol. 15, No. 9, pp. 1312-1314. 2003

37. S. J. B. Yoo, F. Xue, Y. Bansal, J. Taylor, Z. Pan, J. Cao, M. Jeon, T. Nady, G. Goncher, K. Boyer, K. Okamoto, S. Kamei, and V. Akella. HIGH-PERFORMANCE OPTICAL-LABEL SWITCHING PACKET ROUTERS AND SMART EDGE ROUTERS FOR THE NEXT-GENERATION INTERNET. IEEE Journal of Selected Areas in Communications, Vol. 21, No. 7, pp. 1041-1051 2003

38. J. Oliver and V. Akella. IMPROVING DSP PERFORMANCE WITH A SMALL AMOUNT OF FIELD PROGRAMMABLE LOGIC. Proceedings of the 13th International Conference on Field-Programmable Logic and Applications, FPL 2003, LNCS 2779, P.Y.K. Cheung, et al (Eds.), pp. 520-532. 2003

39. F. Xue, Z. Pan, Y. Bansal, J. Cao, M. Jeon, K. Okamoto, S. Kamei, V. Akella, and S. J. B. Yoo. END-TO-END CONTENTION RESOLUTION SCHEMES FOR AN OPTICAL PACKET SWITCHING NETWORK WITH ENHANCED EDGE ROUTERS. IEEE/OSA Journal of Lightwave Technology, Vol. 21, No. 11, pp. 2595-2604. 2003

40. M. Y. Jeon, Z. Pan, J. Cao, Y. Bansal, J. Taylor, Z. Wang, V. Akella, K. Okamoto, S. Kamei, J. Pan, and S. J. B. Yoo. DEMONSTRATION OF ALL-OPTICAL PACKET SWITCHING ROUTERS WITH OPTICAL LABEL SWAPPING AND 2R REGENERATION FOR SCALABLE OPTICAL LABEL SWITCHING NETWORK APPLICATIONS. IEEE/OSA Journal of Lightwave Technology, Vol. 21, No. 11, pp. 2723-2733. 2003

41. J. Cao, M. Jeon, Z. Pan, Y. Bansal, Z. Wang, Z. Zhu, V. Hernandez, J. Taylor, V. Akella, S. Yoo, K. Okamoto, and S. Kamei. ERROR-FREE MULTI-HOP CASCADED OPERATION OF OPTICAL LABEL SWITCHING ROUTERS WITH ALL-OPTICAL LABEL SWAPPING. In the IEEE/OSA Optical Fiber Communication Conference Technical Digest, pp. 791-792. 2003

42. J. Taylor, Y. Bansal, M. Y. Jeon, Z. Pan, J. Cao, V. J. Hernandez, Z. Zhu, Z. Wang, S. J. B. Yoo, V. Akella, T. Nady, G. Goncher, K. Ervin, K. Boyer, and B. Davies. DEMONSTRATION OF IP CLIENT-TO-IP CLIENT PACKET TRANSPORT OVER AN OPTICAL LABEL-SWITCHING NETWORK WITH EDGE ROUTERS. Proceedings of the 29th European Conference on Optical Communication, ECOC-IOOC, Vol. 1, pp. 20-21. 2003

43. Z. Pan, M. Y. Jeon, Y. Bansal, J. Cao, J. Taylor, S. J. B. Yoo, V. Akella, K. Okamoto, and S. Kamei. PACKET-BY-PACKET CONTENTION RESOLUTION IN AN OPTICAL-LABEL SWITCHING SYSTEM WITH 2R REGENERATION. IEEE/OSA Conference on Lasers and Electro-optics Technical Digest, paper CThX6, 2003

44. Z. Pan, H. Yang, Z. Zhu, J. Cao, V. Akella, S. Butt, and S.-J. B. Yoo. EXPERIMENTAL DEMONSTRATION OF VARIABLE-SIZE PACKET CONTENTION RESOLUTION AND SWITCHING IN AN OPTICAL-LABEL SWITCHING ROUTER. IEEE/OSA Optical Fiber Communication Conference Technical Digest, 3 pp. (2004)

45. John Oliver, Ravishankar Rao, P. Sultana , J. Crandall, E.. Czernikowski, LW Jones IV, D. Copsey, D. Keen, Venkatesh Akella, Chong FT. DESIGN OF A TILE-BASED EMBEDDED

ARCHITECTURE. Power-Aware Computer Systems. Third International Workshop, PACS 2003. Revised Papers (Lecture Notes in Computer Science Vol.3164). Springer-Verlag. 2004, pp.73-85. Berlin, Germany. (13 pages)

46. John Oliver, Ravishankar Rao, Paul Sultana, Jedidiah Crandall, Erik Czernikowski, Leslie W. Jones IV, Diana Keen, Venkatesh Akella, and Frederic T. Chong SYNCHROSCALAR: A MULTIPLE CLOCK DOMAIN POWER AWARE TILE-BASED EMBEDDED PROCESSOR, International Symposium on Computer Architecture, ISCA, June 2004 (12 pages)

47. Gouri Landge, Mihaela van der Schaar, Venkatesh Akella, COMPLEXITY ANALYSIS OF SCALABLE MOTION-COMPENSATED WAVELET VIDEO DECODERS Proc. SPIE Vol. 5558, p. 444-453, Applications of Digital Image Processing XXVII; Andrew G. Tescher; Ed. (9 pages)

48. Mihaela van der Schaar, D. Turaga and Venkatesh Akella, RATE-DISTORTION-COMPLEXITY ADAPTIVE VIDEO COMPRESSION AND STREAMING Image Processing, 2004. ICIP '04. 2004 International Conference on,Volume 3, 24-27 Oct. 2004 Page(s):2051 - 2054 Vol. 3 (4 pages)

49. Zhong Pan, Haijun Yang, Zuqing Zhu, Jing Cao, Venkatesh Akella, Steven Butt, S. J. Ben Yoo, DEMONSTRATION OF VARIABLE-SIZE PACKET CONTENTION RESOLUTION AND PACKET FORWARDING IN AN OPTICAL-LABEL SWITCHING ROUTER, IEEE Photonics Technology Letters, vol. 16, no. 4, July 2004.(3 pages)

50. John Oliver, Venkatesh Akella and F. T. Chong. EFFICIENT ORCHESTRATION OF SUBWORD PARALLELISM IN SIMD ARCHITECTURES. Proceedings of the Sixteenth ACM Symposium on Parallelism in Algorithms and Architectures, June 27-30, 2004, Barcelona, Spain, pages 225-234 (10 pages)

51. Fei Xue, Zhong Pan, Haijun Yang, Jinqiang Yang, Jing Cao, Okamoto K, Kamei S, Venkatesh Akella, Yoo SJB. DESIGN AND EXPERIMENTAL DEMONSTRATION OF A VARIABLE-LENGTH OPTICAL PACKET ROUTING SYSTEM WITH UNIFIED CONTENTION RESOLUTION. Journal of Lightwave Technology, vol.22, no.11, Nov. 2004, pp.2570-81. (11 pages)

52. Haijun Yang, Venkatesh Akella, Chen-Nee Chuah, and S. J. Ben Yoo, SCHEDULING OPTICAL PACKETS IN WAVELENGTH, TIME AND SPACE DOMAINS FOR ALL-OPTICAL PACKET SWITCHING ROUTERs, IEEE International Conference on Communications (ICC) 2005, Seoul, Korea, May 2005.

53. Junqiang Hu, Zhong Pan, Zuqing Zhu, Haijun Yang, Tinoosh Mohsenin, Venkatesh Akella, S. J. Ben Yoo, FIRST EXPERIMENTAL DEMONSTRATION OF IP-CLIENT-TO-IP-CLIENT VIDEO STREAMING APPLICATION OVER AN ALL-OPTICAL LABEL-SWITCHING NETWORK WITH EDGE ROUTERS, Optical Fiber Communication Conference, paper OFP2, 2005.

54. Gouri Landge, Mihaela van der Schaar, Venkatesh Akella, GENERIC MODELING OF COMPLEXITY FOR MOTION-COMPENSATED WAVELET VIDEO DECODERS in Image and Video Communications and Processing 2005, Volume 5685, No. 5685, Edited-by Amir Said, John G. Apostolopoulos, pages 347-353. (7 pages)

55. G. Landge M. van der Schaar and Venkatesh Akella, COMPLEXITY METRIC DRIVEN ENERGY OPTIMIZATION FRAMEWORK FOR IMPLEMENTING MPEG-21 SCALABLE VIDEO DECODERS,

Acoustics, Speech, and Signal Processing, 2005. Proceedings. (ICASSP '05). IEEE International Conference on Volume 2, March 18-23, 2005 Page(s):1141– 1144 (4 pages)

56. Venkatesh Akella, M. van der schaar and Wen Fu Kao, PROACTIVE ENERGY OPTIMIZATION ALGORITHMS FOR WAVELET-BASED VIDEO CODECS ON POWER-AWARE PROCESSORS, International Conference on Multimedia & Expo, ICME 2005 (4 pages)

57. Venkatesh Akella and Soheil Ghiasi OVERCOMING VON NEUMANN TO SAVE MOORE, High Performance Embedded Computing Workshop, MIT Lincoln Laboratories, September, 2005

58. Z. Pan, H. Yang, J. Yang, J. Hu, Z. Zhu, J. Cao, K. Okamoto, S. Yamano, V. Akella, and S.-J. B. Yoo. ADVANCED OPTICAL-LABEL ROUTING SYSTEM SUPPORTING MULTICAST, OPTICAL TTL, AND MULTIMEDIA APPLICATIONS. " IEEE/OSA Journal of Lightwave Technology, vol. 23, no. 10, pp. 3270-3281, October 2005.

59. J. Oliver, R. Rao, D. Franklin, F. Chong and V. Akella. SYNCHROSCALAR: EVALUATION OF AN EMBEDDED, MULTI-CORE ARCHITECTURE FOR MEDIA APPLICATIONS. Journal of Embedded Systems: Special Issue on Multi-Core Architectures, December 2005.

60. Darshan D. Thaker, Diana Franklin, Venkatesh Akella, Frederic T. Chong, RELIABILITY REQUIREMENTS OF CONTROL, ADDRESS, AND DATA OPERATIONS IN ERROR TOLERANT APPLICATIONS, First Workshop on Architectural Reliability, Barcelona, 2005.

61. Junqiang Hu, Zhong Pan, Zuqing Zhu, Haijun Yang, Venkatesh Akella, and S. J. Ben Yoo, " First experimental demonstration of combined multicast and unicast video streaming over an optical-label switching network," in IEEE/OSA Optical Fiber Communication Conference (IEEE/OSA OFC 2006), paper OTuJ2, Anaheim, California, March 2006.

62. Ravishankar Rao, Justin Wenck, Diana Franklin, Raj Amirtharajah and Venkatesh Akella, “Exploiting Non-Uniform Memory Access Patterns through Bit-line Segmentation” ACM SIGMICRO Letters Volume 24, Number 1, 2006, 9 pages. (Selected top papers from 4th Workshop on Memory Performance Improvement, WMPI 2006)

63. Ravishankar Rao, Justin Wenck, Diana Franklin, Raj Amirtharajah and Venkatesh Akella, “Segmented Bitline Cache”, High Performance Computing - HiPC 2006, 13th International Conference, Bangalore, India, December 18-21, 2006, Proceedings. Lecture Notes in Computer Science 4297 Springer 2006, ISBN 3-540-68039-X

64. John Oliver and Ravishankar Rao and Michael Brown and Jennifer Mankin and Diana Franklin and Frederic T. Chong and Venkatesh Akella, “Tile Size Selection for Low-Power Tile-Based Architectures”, ACM International Conference on Computing Frontiers, CF06, Ischia, Italy, May 2006

65. John Oliver, Diana Franklin, Fred Chong and Venkatesh Akella “Using Application Bisection Bandwidth to Guide Tile Size Selection for Synchroscalar Tile Based Architecture”, Transaction on High-Performance Embedded Architectures and Compilers, Volume 1, December 2006.

66. Haijun Yang, Venkatesh Akella, Chen-Nee Chuah, and S. J. Ben Yoo, "Design of novel optical router controller and arbiter capable of asynchronous, variable length packet switching," in International Conference on Photonics in Switching 2006 (PS2006), Herakleion (Crete), Greece, October 2006.

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