3D-Transistor Array Based on Horizontally Suspended Silicon Nano-Bridges Grown via a Bottom-up Technique

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Self-assembled semiconductor nanowires, prepared by bottom-up techniques, are touted to be promising building blocks for future nanodevices because they have inherently small dimensions as well as wide choices of materials and compositions. They have been employed in fabrication of a wide range of nanodevices such as field-effect-transistors (FETs),[1] photovoltaic devices,[2] light-emitting-diodes,[3] photodetectors,[4] and sensors.[5] Among various kinds of self-assembled nanowires, silicon (Si) nanowires have been actively studied with an aim of bearing the next generation FETs whose feature sizes will be smaller than a few tens of nanometer.[6] In most cases, self-assembled Si nanowire based FETs have been fabricated via pick-and-place or drop-cast techniques[7] because randomly oriented, self-assembled nanowires present an alignment challenge. For creating nanowire devices, the conventional protocols harvest nanowire ensembles from growth substrates and disperse them on device substrates, and therefore, rigorous alignment processes are required to prepare arrays with these randomly oriented and distributed nanowires. These fabrication techniques, therefore, are incompatible with large integration of devices due to lacks of reproducibility and fidelity.

To address the challenging alignment of self-assembled nanowires for device fabrication, several techniques such as contact printing and dielectrophoresis were invented to create arrays out of randomly distributed nanowires.[8,9] Although relatively simple, the contact printing technique requires elaborate patterns on device substrates to coordinate nanowires, and may result in physical and chemical damages on transferred nanowires during processes thereafter.[10] Dielectrophoresis techniques presented state-of-the-art arrays of well-aligned nanowires in a much more controlled manner.[9] This technique, however, imposes precarious fabrication processes for creating additional metal wires and contacts for applying AC signals to draw and align nanowires into the contacts.

Moreover, difficulty in applying a uniform AC electric field over a large area limits wide applications of this technique.

As a more practical way of overcoming the aforementioned obstacles for the integration of nanowire FETs, in-place growth techniques[10–14] have been proposed. Amongst them, fabrication of Si nanowire bridges is particularly attractive because it allows for direct growth of crystallographically aligned nanowires on pre-patterned semiconductor electrodes[14] as well as their metallurgically robust linkages to the electrodes.[12,15] For FETs, the bridged nanowires are then designated as channels, and source/drain electrodes can be readily patterned along with the pre-patterned electrodes. Consequently, compared to any other methods, this route provides much simpler and more practical ways for preparing aligned nanowires and further fabricating FETs thereof. For instance, He et al.[13] presented a single-Si-nanowire bridge FET, which was ingeniously gated by an electrolyte. Osama et al.,[11] on the other hand, demonstrated multiple-nanowire bridge FETs, modulated by a global gate using a bottom substrate. Both nanowire bridge FETs exhibited excellent FET performance, but the lack of FET operations with individual gate electrodes remains to be addressed.

In this work, we aim to provide a practical and reliable method for integrating surrounding gate nanowires FETs, which can be individually addressable, using a bottom-up technique. We created an array of nanowire air-bridges using the VLS growth technique, followed by a successful fabrication of an ample number of Si nanowire gate-all-around (GAA)-FETs without implementing the tedious nanowire alignment and contact formation processes. The statistical summary of our devices' electrical properties strongly suggest that our technique is suitable for reproducible integration of FETs with precision. Furthermore, non-volatile memory device based on these nanowire GAA-FETs exemplify their potential applications. These results reveal that our technique can improve the production of GAA-FETs and application devices thereof, which have not been easily achievable with alternative approaches that rely on self-assembled nanowires.

Our fabrication scheme allowed for the success of creating a few tens of single or multiple channel GAA-FETs in an array. **Figure 1** shows the schematic fabrication process as well as images of a single channel GAA-FET, where only one nanowire bridge was formed between a pair of electrodes without any treatment for removing extra un-bridged nanowires or nanowires grown on the Si electrode surfaces.

Experimental measurement revealed that the single nanowire GAA-FET has the current-voltage characteristics of a typical FET, as exhibited in **Figure 2**a. Source current (I_S) versus gate voltage (V_{GS}) curves collected for three drain voltages (V_{DS}) and gate current (I_{Gate}) versus V_{GS} indicate that the GAA-FET operates in the p-type accumulation mode with

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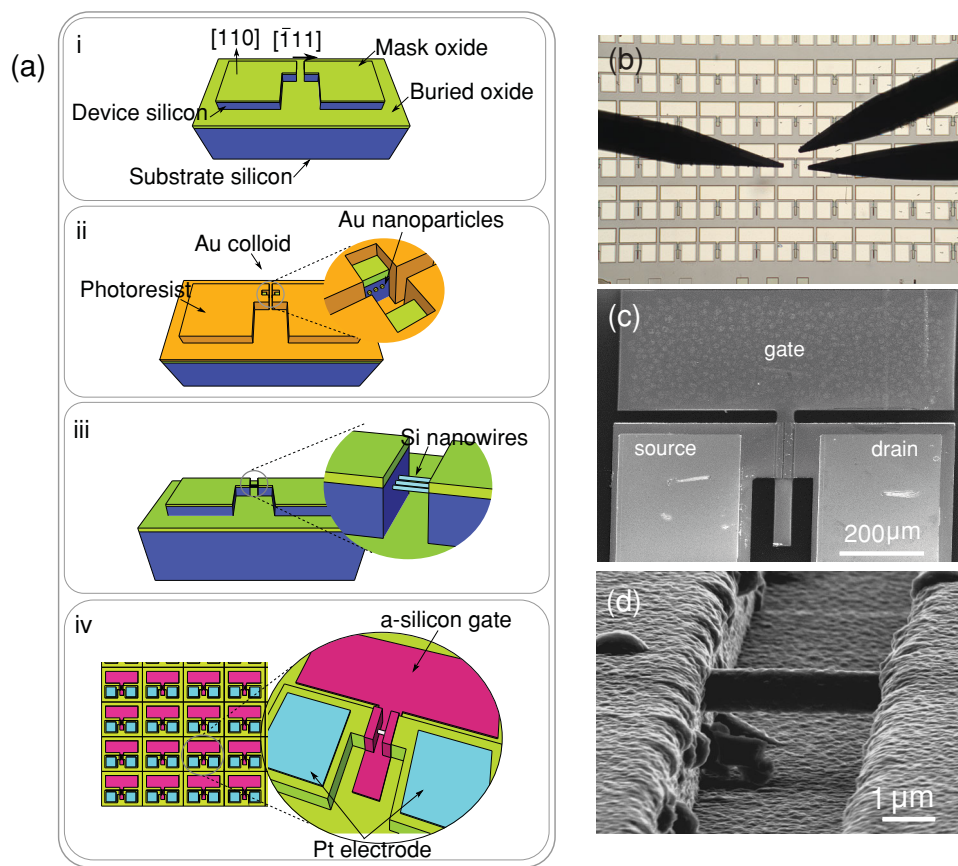Seoul, 139–701, Republic of Korea

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Figure 1. (a) Process flow diagram of integrating nanowire GAA-FETs in an electrode array: i) Si electrode array patterning, ii) Au colloid deposition, iii) Si NW growth, and iv) FET array after electrode deposition (b) Optical microscope image of a GAA-FET array with three probe pins. (c) and (d) SEM micrographs of a single nanowire GAA-FET. Note that a nanowire channel is suspended over a pair of electrodes and surrounded by the amorphous silicon gate.

relatively small gate leakage current. Output current characteristics, drain current (I_D) versus drain voltage (V_{DS}), shown in Figure 2b, also displayed a typical p-channel MOSFET behavior. A threshold voltage shift for different drain voltages, so called, drain-induced-barrier-lowering (DIBL),[16] was 72 mV/V, and an inverse subthreshold swing (SS) was 146 mV/dec. These electrical properties are comparable to those reported for other Si nanowire FETs.[17–19]

Relatively low on-current of the GAA-FET is attributable to a high series resistance along the source and drain. Although we confirmed that Pt contacts on the Si electrodes form good Ohmic contacts with a contact resistance as low as ~255 Ω, a resistance of moderately doped, p-type (~5 × 10^{18} cm^{-3}) Si electrode itself and the large distance from the nanowire/electrode interface to Pt contacts play a major role in voltage drops at the source/drain. Also, long nanowire length (>3 µm) accounts for the increase of the series resistance. Since hole mobility of a <111> Si nanowire is comparable to or slightly higher than those of <100> or <110> nanowires,[20,21] it may not critically deteriorate performance of the GAA-FET. Rather, one of possible reasons for the current reduction is a carrier mobility decrease due to the deep-level trap states created by gold impurities.[22]

Carrier mobility of the GAA-FET was extracted using the current-voltage equation,[23] given by $\mu = \frac{dI_S}{dV_{GS}} \cdot \frac{L^2}{C_{gate} \times V_{DS}}$, where C_{gate} is gate capacitance, L is channel length. Here, due to their low magnitudes, gate capacitances of the nanowire GAA-FETs could not be obtained directly using the typical capacitance-voltage measurement at room temperature.[24] Instead, they were calculated with the equation for a cylindrical capacitor, $C_{gate} = \frac{2\pi\varepsilon_{ox}L}{ln\left(\frac{r+t_{ox}}{r}\right)}$, where ε_{ox} is permittivity of gate oxide, r is a radius of nanowire channel, and t_{ox} is gate oxide thickness. For a calculated capacitance value of 9.6 fF for a nanowire GAA-FET having a 3 µm long and 120 nm thick channel with 10 nm thick gate oxide, the maximum hole mobility in the triode region was estimated to be about 50 cm^2/V for both a low ($V_{DS} = -50$ mV) and a high channel electric fields ($V_{DS} = -1$ V). In this calculation, since we ignored series resistance including resistance of Si electrodes as well as contact resistance at the source/drain electrodes, and assumed Ohmic connections between the nanowires and the electrodes, it should be noted that the calculated mobility value could be the lower bound. The mobility value is within a reasonable range, compared to reported mobilities of 20–510 $cm^2/V·s$ in silicon nanowire FETs.[19,25–28]
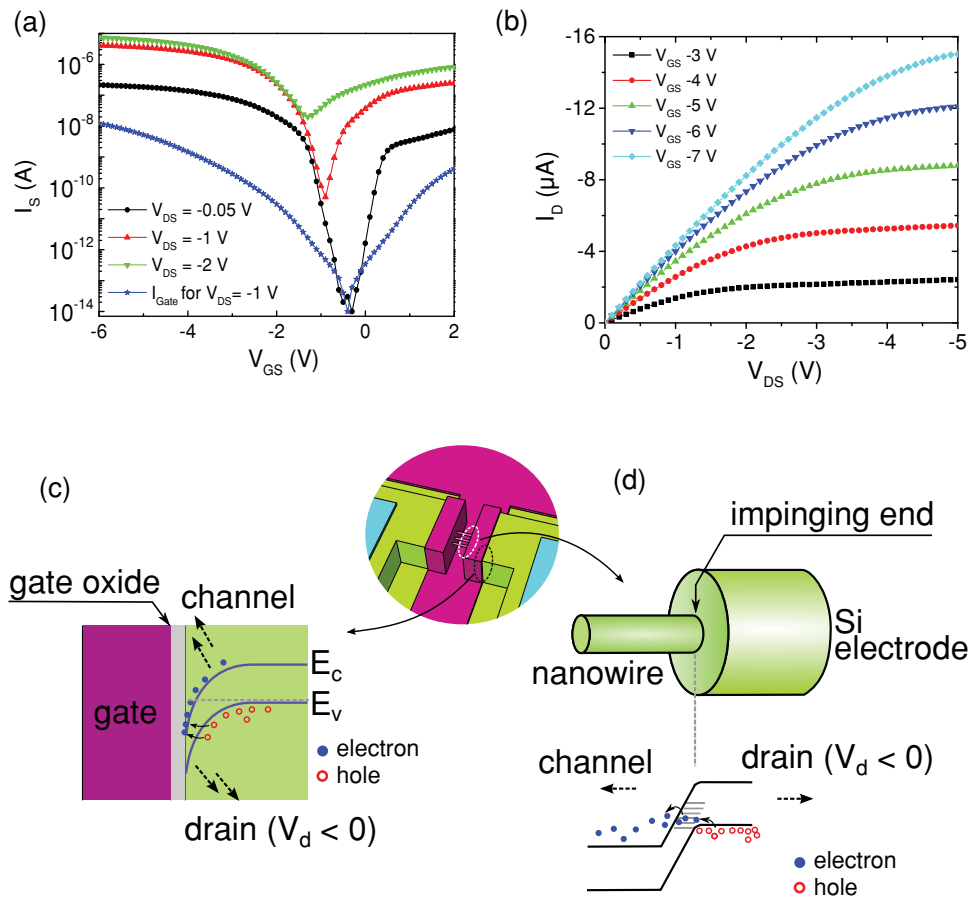
Figure 2. (a) Measured current (I_S)- voltage (V_{GS}) for three drain voltages (V_{DS}). (b) Output characteristics (I_D-V_{DS}), collected from a nanowire channel GAA-FET with a 3 μm long and 120 nm thick channel. An SEM micrograph of this FET is exhbited in Figure 1d. Diagrams of off-current models: (c) Gate-induced-drain-leakage (GIDL) due to band-to-band tunneling at the overlapping areas between the gate and the drain electrodes. (d) Trap-assisted tunneling at the nanowire-electrode junction interface.

Compared to the conventional planar gate FETs, multiple gate FETs—such as tri-gate, pi-gate, Ω-gate, and surrounding gate FETs—have improved controllability over the channel[29,30] in such a way that they effectively suppress the off-current. Owing to enhanced gate controllability, multiple gate FETs aid low power consumption and downscaling of CMOS devices. Although our nano-bridge GAA-FETs have surrounding gates, off-current significantly increased as V_{DS} increases: i.e., minimum off-current of 0.01, 50 and 200 pA for V_{DS} = –0.05, –1 and –2 V, respectively. When off-current increases, on/off-current ratio accordingly decreased from 1×10^7 to 8×10^4, and to 3.5×10^2.

The high off-current comparable to on-current for the nanowire GAA-FET resembles so-called ambipolar characteristics of Schottky-barrier MOSFETs, where Schottky metal contacts are formed on low-doping source/drain regions.[31] In the GAA-FETs, however, nanowire-Si electrode connections and Pt on Si electrodes were confirmed to form Ohmic contacts. Besides, minority carriers (electron) generated by the strong inversion for positive V_{GS} can hardly account for the off-current increase because of the absence of electron injection from p+ Si source/drain electrodes, which was exhibited in other nanowire FETs.[32] Instead, an increase of off-current with gate voltages is attributable to gate-induced-drain-leakage (GIDL)[33,34] and,

if any, trap-assisted tunneling at the nanowire impinging junction.[35] Since a gate-drain overlap area in the GAA-FET is more than 5000 times larger than the nanowire cross-section area, GIDL is anticipated to attribute to the high off-current. Detailed leakage current models are illustrated in Figure 2c and 2d and explained further in the supporting information.

The presented technique has a high potential for producing nanowire FETs because it copes with growing epitaxially aligned nanowires at pre-defined electrodes. In a batch process, we obtained 35 working devices amongst 45 FETs (an effective yield of 80%) in an array. Since this technique depends on the platform of nano-bridges, arrays with high-yield nano-bridges should be achieved for integration of nanowire FETs. To improve the yield of nano-bridges, recently, the technique has been further explored by in-depth investigation to correlate bridging yields and numbers of nano-bridges.[36]

Cumulative probability charts, plotted in **Figure 3**, also explicitly manifest the potential of our technique for integrating multiple nanowire FETs. The charts exhibit threshold voltages ranging from -1 V to -2.6 V; subthreshold slopes from 100 mV/dec to 500 mV/dec; minimum off-current for V_{DS} = -1 V from 3×10^{-13} to 2×10^{-7} A; and on/off-current ratio from 10 to 5×10^6. Median values (at a probability of 50%) of threshold
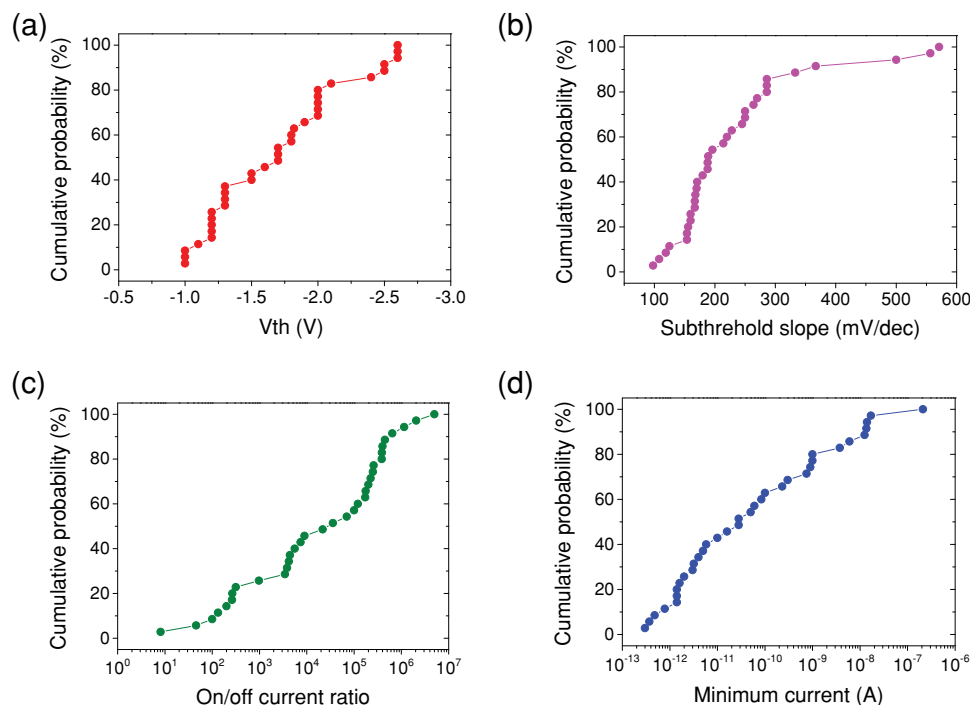
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Figure 3. Cumulative probability plots for (a) threshold voltages, (b) inverse subthreshold slopes (c) on/off current ratios, and (d) minimum off-current for $V_D = -1$ V, collected from the whole thirty five GAA-FETs in the array. I_S -V_{GS} curves collected from thirty GAA-FETs are summarized in Figure S1.

voltages, subthreshold slopes, minimum current, and on/off-current ratio were, respectively, −1.7 V, 188 mV/dec, 2.8×10^{-11} A, and 3×10^4. The wide distribution of minimum off-current and on/off-current ratio should be attributed to structural imperfections such as defective nanowire linkages to electrodes and degraded morphology of electrode surfaces, causing significantly increased GIDL and trap assisted tunneling currents. However, the currently wide distribution of the parameters has room for improvement through more optimized processes for preventing growth of kink-free nanowires, controlling the number of nanowires, and developing atomically smooth connections between nanowire bridges and electrodes.

To demonstrate the potential of our nano-bridge GAA-FETs, variable-oxide-thickness (VARIOT) type nonvolatile memory cells were realized as illustrated in **Figure 4**a.[37] Compared to planar type FETs, nanowire GAA-FETs possess several advantages for improving performance of nonvolatile memory devices. For example, the enhanced electric field applied in the tunneling oxide improves speeds of programming and erasing.[38] Enhanced driving current owing to the current channel formed along the nanowire's entire surface augments the sensing speed and margin.[39] Furthermore, vertical stacks of individually addressable nanowires can boost the integration density of memory devices.[40,41]

The nanowire memory cells could carry out low-voltage programming and erasing operations. As shown in Figure 4b, 10 ms of programming and erasing by three pairs of voltages (±7, ±8, and ±9 V) resulted in memory windows, i.e. threshold voltage shifts, as large as 0.44, 1.2, and 2.5 V, respectively. Such large memory windows by low voltage programming and erasing are comparable to those of high performance nanowire memory devices published elsewhere.[6,38,42,43]

In VARIOT type memory cells, tunneling barriers are engineered to improve programming and erasing speeds as well as charge retention. Energy bands of the tunneling barrier, as illustrated in Figure 4c and 4d, are supposed to bend such sharply in both program and erase operations that electrons can easily tunnel through the barriers.[44] On the other hand, when the gate is grounded or applied lower voltages than ±7 V on, considerably high barriers exist for electrons to tunnel through. In this case, the memory cell can remain undisturbed from additional charges transferred between the channel and the HfO$_2$ layer.

Despite the low voltage operation, the nano-bridge memory cells exhibited low immunity against program/erase cycle stress. Within less than 10–20 times of program/erase operation cycles, gate-source (or gate-drain) leakage current significantly soars and all the memory devices failed to work. This undesirable property of extremely low cyclic operation is tentatively attributed to strong field enhancement at the edge of nanowire linkages on the electrodes and unlinked nanowires, and rough nanowire surfaces. Considerably high electric field causes oxide percolation, which results in generation of leakage current paths through the tunneling barriers.[45,46] Thus, reliability tests such as retention time measurement, stress induced leakage current, and program/erase cycle acceleration tests, could not be implemented.

Lastly, we suggest a few schemes for scaling the nano-bridge GAA-FETs and improving their performance. To increase on-current, the channel length should be decreased
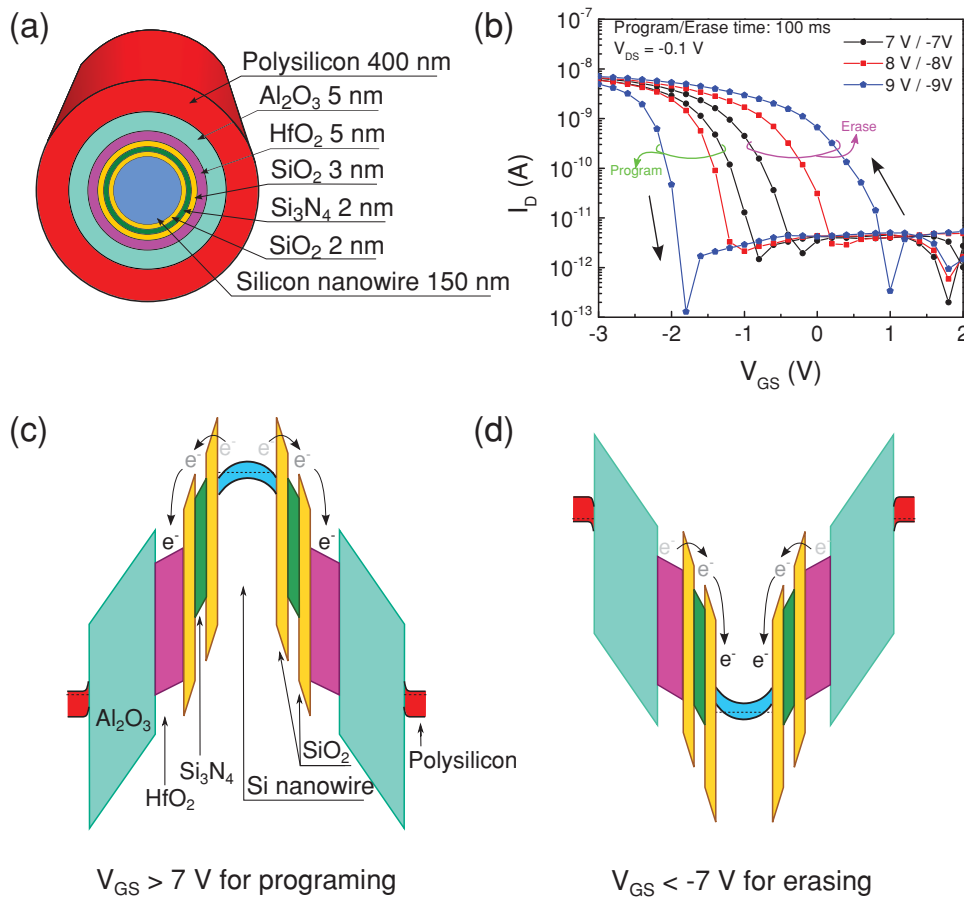
Figure 4. (a) Schematic diagram of the nanowire channel with tunneling barriers, trap layers and the gate in a VARIOT type nanowire air-bridge memory cell, (b) Semi-logarithmic plot of current ($|I_D|$) versus V_{GS} after program and erase operations. For ± 7 V, ± 8 V, and ± 9 V sweeps at $V_{DS} = -0.1$ V, memory window range increases from 0.5 V to 1.3 V and to 2.7 V, respectively; arrows represent sweep/hysteresis direction. Energy band diagrams of the memory cell for (c) programming and (d) erasing.

by implementing electrodes with smaller gaps or by patterning the shorter gate between the electrodes. Silicidation of Si electrodes can significantly diminish series resistance of the GAA-FETs.[47] Stacking multiple nanowires is a good strategy for enhancing on-currents as well as increasing the integration density. Growing thin nanowire bridges and thinning them further by oxidation or wet etching[48] would be beneficial to suppress off-current. One significant advantage of our nano-bridge approach is its scalability and the potential of the heteroepitaxial nanowire on Si despite large lattice mismatches. Hence, integration of high mobility III–V nanowires such as InGaAs[49] or InAs[50] on the Si platform will enable the next generation high performance nanowire FETs.

In conclusion, an array of GAA-FETs with Si nano-bridge channels grown via a bottom-up (VLS) technique has been demonstrated. The horizontally aligned nano-bridges led to the integration of nanowire GAA-FETs without rigorous processes for aligning and contacting the nanowires. The devices exhibited high on/off-current ratios, low subthreshold swings and off-current. Statistical evaluation on electrical properties of the GAA-FETs confirmed that the presented fabrication method possesses a promising capability of integrating nanowire FETs.

In addition, the demonstration of the low voltage operational VARIOT type non-volatile memory cells reveals that our device fabrication scheme has high versatility to prepare other functional nano-devices beyond FETs. These results indicate that horizontally self-aligned nano-bridges can become practical building blocks for producing competitive nanowire-based devices.

Experimental Section

Source/drain silicon electrodes were patterned on p^+-(110) silicon (5×10^{18} cm^{-3}) in SOI, using KOH solutions or reactive ion etching after photolithography. On the sidewall surfaces, photolithography was carried out to create small openings, where nanowires are expected to grow. In those openings, the poly-L-lysine was treated and then gold colloids (200 nm, from Sigma Aldrich), as a catalyst to aid nanowire growth, were deposited. Consecutively, the substrates were cleaned with acetone, a piranha solution ($H_2SO_4:H_2O_2::2:1$), HF acid, and DI water. Silicon nanowires were grown via the vapor-liquid-solid (VLS) technique using a cold-wall chemical-vapor-deposition tool (First Nano®) with SiH_4, B_2H_6, HCl, and H_2 gases. Growth temperature and pressure were respectively 575 °C and 13 torr. Diameters and lengths of nanowires were determined by sizes of gold nanoparticles and growth time,

respectively. Gold tips and impurities along silicon nanowire surfaces were removed using a gold etchant TFA (from TRANSENE company inc.) without damaging the nanowires prior to additional processes. Detailed procedures for creating nanowire bridges are presented in our previous work.[36] For creating GAA-FETs, the nanowire bridges, were oxidized at 900 °C for 10 min to grow 10 nm thick gate oxide. On the oxidized nanowires, p+ amorphous silicon was conformally deposited and delineated to the gate electrodes using photolithography and wet etch. The detailed process flow is schematically illustrated in Figure S1 in the supporting information. For fabricating flash memory cells, on the other hand, tunneling barrier layers of SiO_2 (2 nm)/Si_3N_4 (3 nm)/SiO_2 (2 nm), a charge trap layer of HfO_2 (5 nm), and a blocking layer of Al_2O_3 (15 nm) were sequentially deposited on nanowire bridges. The detailed deposition scheme and structural analysis of the tunneling barrier are presented elsewhere.[44] Using the lift-off technique, platinum thin film pads were fabricated to create Ohmic contacts on the silicon electrodes. Micrographs of the FETs were collected using a scanning electron microscope, FEI XL30. Electrical properties of devices were characterized by Agilent 4156C in ambient conditions.

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Supporting Information

3D-Transistor Array Based on Horizontally Suspended Silicon Nano-bridges Grown via a Bottom-up Technique

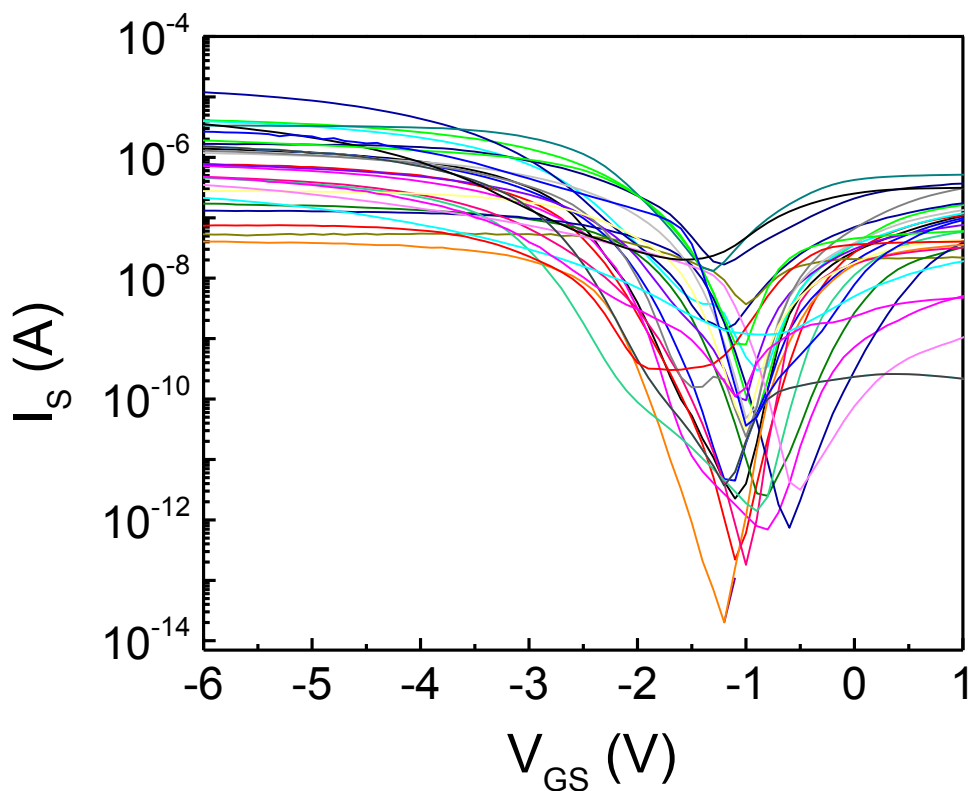*Jin Yong Oh, Jong-Tae Park, Hyun-June Jang, Won-Ju Cho, and M. Saif Islam**

Figure S1. Summary of I_S-V_{GS} (V_{DS} = -1 V) measurement data for 30 nanowire GAA-FETs' threshold voltages, inverse subthreshold swings, on/off current ratio, minima current are summarized in Figure 3.

In our devices, we hypothesize that the GIDL current significantly rises because the gate electrode overlaps source/drain electrodes in a significantly large area. At the surface below the overlap area, a narrow depletion region is created due to a large potential difference between the gate and drain. Strong band bending in the depletion region, as illustrated in Figure 2c, causes band-to-band tunneling of carriers.[1] Since the nanowire channels of the GAA-FETs are suspended in the air across a pair of thick Si electrodes, surrounding gate cannot help covering source/drain electrodes as well as the channel. Compared to the cross-sectional area of the channel, the overlapping area is more than three orders of magnitude larger; consequently, off-current gets significantly increased.

High density surface states at the nanowire impinging junction can lower tunneling barrier, and therefore render off-current increasing, as illustrated in Figure 2d. Using low pressure CVD, Si electrode surfaces are oxidized during the nanowire synthesis.[2] Although gold contamination was not detected at the nanowire impinging junction in Ref. 2, it should be taken into consideration because gold impurities are incorporated in nanowire surfaces during the nanowire synthesis.[3] High density surface states due to native oxide and metal impurities at the interface between the nanowire channel and electrodes may cause trap-assisted tunneling, as evident by the device simulation results for FETs with Si/InAs nanowire junction.[4]

Off-current can be controllably reduced for our nanowire-air bridge GAA-FETs, however. For instance, GIDL current will be lessened by implementing thin and narrow source/drain electrodes to which nanowire bridges link and narrower gate electrodes than the channel length to eliminate overlaps with source/drain electrodes. In addition, the off-current via trap assisted tunneling can be suppressed when native oxide growth is prevented by synthesizing nanowires in

a high vacuum as well as by using CMOS friendly metals catalysts such as copper and titanium

to catalyze Si nanowire growth, to allow shallow traps in the silicon bandgap.

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