ACS Photonics

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pubs.acs.org/journal/apchd5

High Speed Surface Illuminated Si Photodiode Using Microstructured Holes for Absorption Enhancements at 900−1000 nm Wavelength

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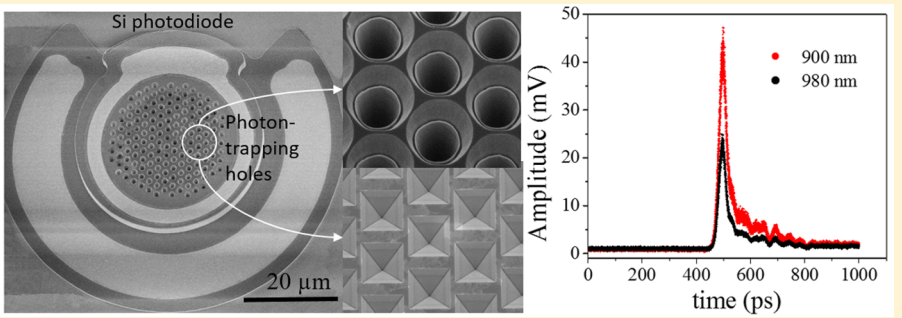
Supporting Information



ABSTRACT: A surface-illuminated silicon photodiode with both high speed and usable external quantum efficiency from 900 to 1000 nm wavelength is highly desirable for intra/inter data center Ethernet communications, high performance computing, and laser radar application. Such Si photodiodes have the potential for monolithic integration to CMOS integrated circuits which can significantly reduce the cost of data transmission per gigabit below one US dollar. To overcome silicon's intrinsic weakness of absorption in these wavelengths, photon-trapping microstructured hole arrays are etched into the silicon surface, and the operational wavelengths of a high-speed silicon PIN photodiode are extended to 1000 nm. In this paper, the design and fabrication of such photon-trapping structures integrated into all-silicon photodiodes with significantly reduced absorption layer thicknesses to achieve high external quantum efficiency and fast response are presented. Different designs and geometries of the submicron holes on the silicon surface can affect the light trapping and ultimately contribute to different external quantum efficiencies at these wavelengths. Some designs are capable of enhancing the absorption by more than an order of magnitude compared to a photodiode without the submicron hole arrays. With the silicon *i*-layer thickness less than or equal to 2 μm, the all-silicon photodiode with integrated submicron holes exhibited an external quantum efficiency of more than 40% at 900 nm and greater than 15% at 1000 nm. This thin absorption layer also allows the fast speed of the photodiode with temporal responses of ∼30 ps at these wavelengths.

KEYWORDS: *photon-trapping, microstructure holes, high quantum efficiency, high speed, all-silicon photodiode*

With increasing data rates of 10, 25, 50, and 100 Gb/s and beyond, the use of a single wavelength at 850 nm for short reach optical data communication cannot satisfy the demands of modern data centers and high performance computing (HPC). Short wavelength division multiplexing (SWDM) is becoming more common as many as 4 to 5 wavelength ranges are piped into a single multimode optical fiber.[1,2] The wavelengths can range from 850 to 940 nm, for example, 850, 880, 910, and 940 nm, according to the Multi Source Agreement for 100 Gb/s Ethernet application.[3−6] An additional wavelength at 980 nm was also proposed.[4] Another application is HPC systems, which covers wavelengths of 990, 1015, 1040, and 1065 nm.[5,7,8] In addition, laser radar (LIDAR or LADAR) systems use a wide range of wavelengths, for example, 850 and 905 nm for automobile application[9] and 1065 nm for 3D topographic imaging application.[10] In the optical link systems, the traditional photodiode of choice is an AlGaAs/GaAs or InGaAs/InP photodiode. Such photodiodes are made from direct bandgap materials and offer high external

Received: May 14, 2017
Published: July 18, 2017

DOI: 10.1021/acsphotonics.7b00486
ACS Photonics XXXX, XXX, XXX−XXX

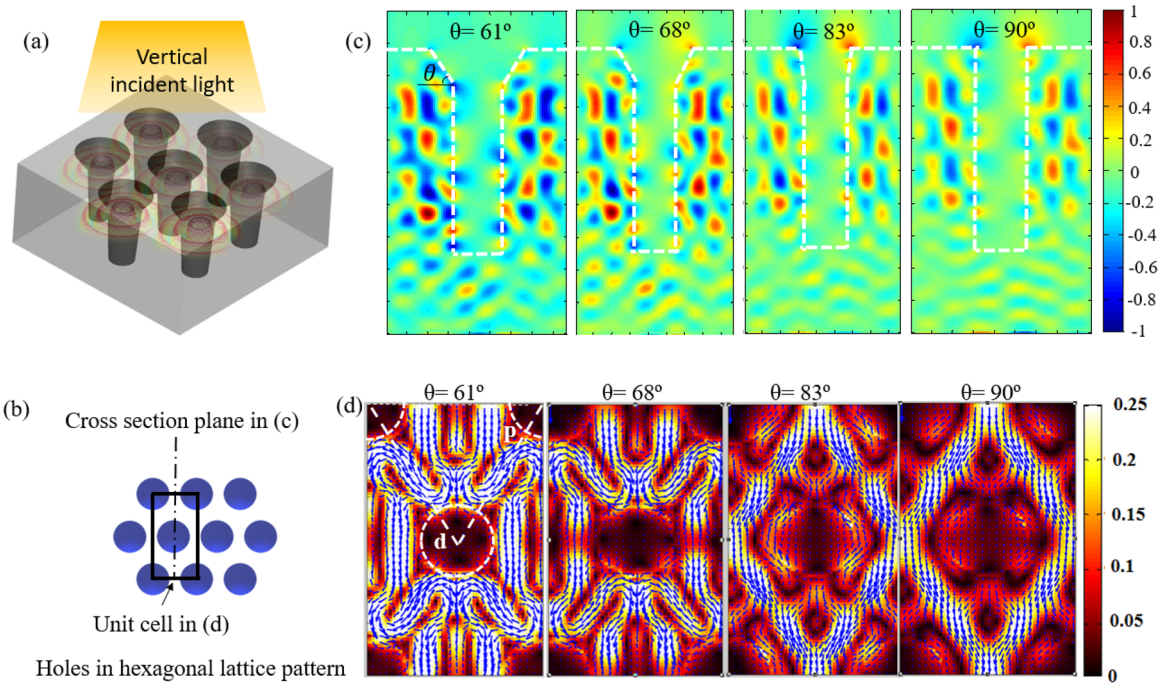


Figure 1. (a) Schematics showing that the vertical incident light transforms to lateral propagating waves in silicon enabled by the periodic submicron holes; (b) Schematics of holes in hexagonal lattice pattern, showing the location of cross-section plane for simulation in (c) and the unit cell in (d) which consists of a complete hole in the center and four 1/4 of holes in the corners; (c) FDTD numerical simulations showing the normalized electric field density distribution around the cross-section of the funneled holes with different sidewall angles (61°, 68°, 83°, and 90°) under top illumination with a wavelength of 980 nm. The white dashed lines represent the boundaries of the holes, and the color scale represents the normalized electric field distribution; (d) Top view of poynting vectors of the light energy around the holes with different angles under vertical optical illumination at the wavelength of 980 nm after 104 fs. The blue arrows represent the energy flux direction and the color scales represent the normalized energy flux densities. White dashed circles represent the boundaries of the submicron holes, "d" represents the diameter of the submicron holes, and "p" represents the period between the submicron holes. The absorption *i*-layer thickness is 2 μm in (c) and (d).

quantum efficiencies (EQE). However, they cannot be monolithically integrated with silicon and require hybrid integration such as wafer bonding and wire bonding in order to be integrated into silicon (Si) electronic chips.[11] None of the integration techniques are conducive to high volume production on 12 in. silicon wafers.

Silicon photodiodes are not used traditionally due to its weak absorption coefficient at the near-infrared wavelengths close to silicon bandgap wavelength (1.1 μm). At 300 K, the absorption coefficient of silicon drops from 4140 cm^{-1} at the wavelength of 600 nm to just 535 cm^{-1} at the wavelength of 850 nm, and further to 95.9 cm^{-1} at the wavelength of 980 nm.[12] These optical properties have limited the application of silicon photodiodes mostly in the visible and near-infrared wavelength regime with a bandwidth of less than 3 Gb/s. For the wavelengths longer than 800 nm, a conventional PIN Si photodiode would need an *i*-layer thickness of more than 10 μm to exhibit a reasonable EQE.[13−17] However, in the current silicon photodiode technology, high speed and high efficiency are often a trade-off, since a high-speed device needs thin "intrinsic" absorption layer to reduce the electron−holes pair transit time. To overcome this dilemma, the effective absorption of Si needs to be enhanced without increasing the intrinsic layer thickness to maintain the high-speed performance of the Si photodiodes of 10−25 Gb/s.

Solar cells with micro- and nanostructures have been demonstrated with enhanced absorption[18−25] and the conversion efficiency improvement by 20−25%[19,20,23] using photon-trapping techniques. A high speed high efficiency Si PIN photodiode with microstructure holes was also demonstrated at 850 nm.[26] In this work, wavelengths of 900−1000 nm are addressed and this spectrum is only 100 nm from the band edge of Si. The all-silicon photodiode has the ability to cover all the wavelengths for SWDM applications for 100 Gb/s Ethernet applications, part of the wavelengths for HPC applications and all the wavelengths for automobile LIDAR systems. The quantum efficiency of a silicon photodiode with microstructure holes can be 500% to over 1000% improvement over a similar PIN photodiode without absorption enhancement micro and nanostructures. The clear advantage of silicon photodiodes is the ability for monolithic integration with CMOS electronics such as transimpendance amplifiers (TIA),[27−29] for example. In this paper, the focus is on the design and fabrication aspects of the photon-trapping submicron structures. Different etch methods used to create different shapes and depths of the submicron holes are studied to maximize the EQE of the device. Both simulations and experiments results show that the physical design parameters of the submicron holes including the geometry, the periodic lattice constant, sizes, sidewall angles, and device surface, all collectively affect the photon trapping capability, thus, result in different EQEs for the same intrinsic layer thickness.

RESULTS AND DISCUSSION

Theory and Simulations. In the previous work,[26] it has been shown that due to the 2D periodic holes on the silicon surface, the initial incident vertical plane waves transform to an ensemble of lateral collective modes, and thus, enhance the effective optical path for absorption. This is analogous to the

DOI: 10.1021/acsphotonics.7b00486
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generated ripple waves as pebble is dropped into a still pool of water. The schematics of the photon-trapping mechanism is shown in Figure 1a. Funnel-shaped holes are used in the simulation in this work to reflect the actual etch geometry of the holes from the fabrication process as will be described later in this paper. Different opening angles (indicated as shown in Figure 1b) of the funnel-shaped holes are simulated by applying finite-difference time domain (FDTD) method. A plane-wave (λ = 900−1000 nm) source is incident on the structures from the top. To model the infinite periodic arrays of nanostructures, periodic boundary conditions (PBC) are used at the lateral boundaries; while perfectly matched layers (PML) are used for top and bottom walls of simulation region. To calculate the absorption, light reflection $R(\lambda)$ and transmission $T(\lambda)$ are obtained from the hole arrays, and the absorption can be achieved by $A(\lambda) = 1 - (T(\lambda) + R(\lambda))$. Only simulations of the funnel shaped holes are presently here, with a diameter (d) of 700 nm, and a period (p) of 1000 nm in 2D hexagonal lattice pattern, as shown in Figure 1b. The holes are 2.5 μm deep and consist of 2 μm absorption intrinsic "i" layer.

Figure 1c shows that, regardless of the opening angles, the periodic holes arrays can support a set of modes in both vertical and lateral directions at wavelength of 980 nm. Figure 1d shows that at the wavelength of 980 nm, the poynting vector is directed laterally from the holes into adjacent silicon, which means that the light propagates in the lateral direction and then remains confined in Si until it gets absorbed. Since our photodiodes have much larger diameters (30−100 μm in the lateral direction) than the i-layer thickness (vertical direction), the laterally propagating waves can be absorbed efficiently for wavelengths between 900 and 1000 nm. The EQE of the holes based photodiodes, thus, can be greatly enhanced compared to the device without photon-trapping holes. It should also be noted that both electric fields and poynting vectors simulations point out the potential advantages of using holes with smaller sidewall angles: the normalized electric filed and energy flux density are stronger in holes with smaller sidewall angles (61° and 68°) compared to the ones with larger sidewall angles (83° and 90°).

To compare with the experimentally measured EQE, the absorption only taking place in the 2 μm i-layer region is considered as the simulated EQE values in these photodiodes. Figure S1 in the Supporting Information, section S1 illustrates the simulated EQE of the photodiodes with funneled holes of different opening angles at the wavelengths between 900 and 1000 nm. It is predicted that by employing the submicron holes, it can significantly improve the EQE by an order of magnitude and extend to the wavelength range of reasonably high EQE even at 1000 nm compared to the photodiodes without any photon-trapping holes.

Designs of the Photon-Trapping Holes Based All-Silicon Photodiode. The all-silicon photon-trapping holes based photodiodes have a PIN mesa structure with n-Si as the top layer and p-Si as the bottom layer as shown in Figure 2a. Different designs of the holes are included in our photodiodes: (1) the submicron holes are in two different lattice patterns: square lattice as shown in Figure 2b and hexagonal lattice, as shown in Figure 2c; (2) the holes have six different designs of diameters (d) and periods (p): (I) d/p: 1300/2000 nm, (II) d/p: 1500/2000 nm, (III) d/p: 700/1000 nm, (IV) d/p: 630/900 nm, (V) d/p: 1500/2500 nm; (VI) d/p: 1300/2300 nm; (3) different shapes of the holes are created by nanofabrication dry etch, wet etch and their combination as will be explained later

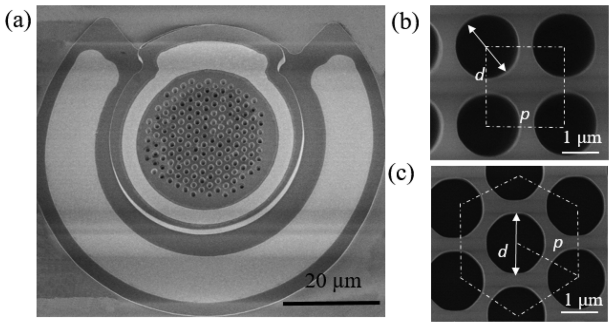

Figure 2. (a) SEM images of submicron holes based all-silicon photodiodes with mesa structures (the thinner ring is n-ohmic metal on n-mesa, and the thicker opened ring is the p-ohmic metal on p-mesa). (b) Top view SEM image of patterned holes in square lattice. (c) Top view SEM image of patterned holes in hexagonal lattice. The white dashed lines in (b) and (c) represent the lattice lines in a unit cell, "d" represents the diameter of the submicron holes, and "p" represents the period between the submicron holes.

in this paper. These different designs are compared to obtain the optimal performance of the photodiodes at wavelengths between 900 and 1000 nm.

The photodiodes' PIN layers are epitaxially grown on the 0.25 μm thick p-type device layer on a SOI substrate. The device response time with respect to delta-function-like input light illumination is limited by (1) the electron and hole drift process inside the i-layer ($\sim 10^1$ ps) and (2) the minority carrier diffusion and recombination processes in the p- and n-layers ($\sim 10^2$ ps). To reduce the minority carriers' lifetime and make the recombination faster in (2) resulting in faster device response, both n and p layers are heavily doped. A boron-doped (5×10^{20} cm^{-3}) SiGeB layer is used as a p-type contact layer (labeled as p+ layer in Figure 3), and a phosphorus-doped (10^{19}

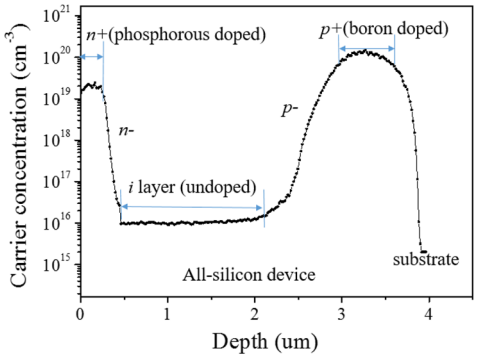

Figure 3. Carrier concentration profile of the fabricated photodiode device measured by two-point spreading resistance technique. The intrinsic layer thickness is less than the designed 2 μm due to the dopant diffusion from highly doped p+ and n+ layers.

cm^{-3}) Si layer is used as an n-type contact layer (labeled as n+ layer in Figure 3). The i-layer is left undoped but turned out to be very slightly n-type doped ($\lesssim 5 \times 10^{16}$ cm^{-3}) in our devices. The i-layer has a designed thickness of 2 μm, but due to the diffusion of the dopant atoms from n+ and p+ layers, transition layers are formed next to the i layer (labeled as n- and p- in Figure 3, respectively). They are 0.2 and 0.65 μm thick, respectively, and result in reduced thickness of the i-layer (<1.6 μm). Fortunately, it does not cause any serious problem in this initial series of experiments reported in this paper.

DOI: 10.1021/acsphotonics.7b00486
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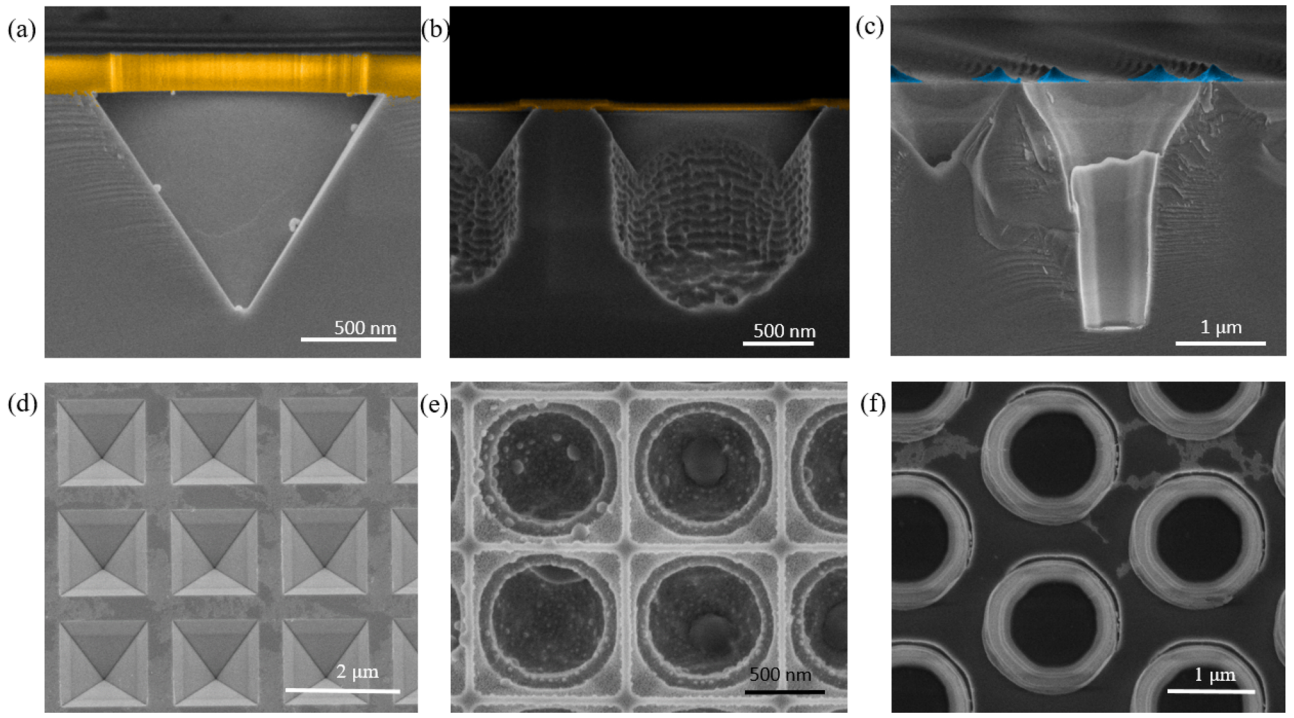

Figure 4. Cross-sectional SEM images of (a) holes with sidewall angle of 54.7° by wet KOH etch with 300 nm patterned PECVD silicon nitride hardmask (in brown color); (b) holes by wet KOH etch followed by DRIE dry etch with 60 nm patterned PECVD silicon nitride hardmask left on the surface (in brown color). The tapering angle of the holes at the opening is created by KOH, and the straight sidewall is created by DRIE; (c) 3 μm deep holes etched by RIE with pyramid shaped DUV resist (in blue color) formed at the holes spacing. (The design of the holes is 1300 nm in diameter and 2000 nm in period (d/p = 1300/2000 nm) arranged in square lattice in (a) and (b), and in hexagonal lattice in (c).) (d–f) Top view SEM images of (a)–(c), respectively (the hardmask or resist are stripped in d–f).

Creating Submicron Holes with Different Geometries and Sidewall Angles. Different etching techniques have been employed to create different geometries and sidewall angles of the submicron holes. The straight submicron holes, as shown in Figure S2, were created using deep reactive ion etch (DRIE), and the details are presented in Supporting Information S2. Isotropic dry etch (SF_6-based DRIE etch)[30−33] as shown in Figure S3(a) and silicon isotropic wet etch ($HNO_3/H_2O/NH_4F$ mixed solution)[34,35] as shown in Figure S3(b) can create shallow tapered holes by enabling an undercut beneath the hardmask. The nature of the isotropic etch can easily cause the adjacent holes to interconnect with each other, especially in the holes with smaller periods. These interconnecting holes contribute to a significant materials loss on the sidewall and lead to very low EQEs of the device. This is because the spacing between the holes becomes very thin and any electron–hole pair generated experience higher resistance in constricted structures where surface depletion can impose additional constraints on the transport characteristics.[34]

KOH anisotropic wet etch can form inverted pyramid-shaped holes with a fixed sidewall angle of 54.7° in the (1 0 0) silicon wafer as Figure 4a shows. The intersection of the (1 1 1) plane causes a self-limiting etch and thus the depths of the different holes are determined by the diameter of the holes as Table S1 shows in the Supporting Information S4. In addition, due to the etch rate difference in (1 0 0), (1 1 0), and (1 1 1) planes,[36] the KOH wet etch makes undercut under the silicon nitride mask and forms square inverted pyramid shaped holes as Figure 4d shows even the hardmask pattern is circular.

To extend the depth of the holes by KOH wet etch, another DRIE dry etch is employed after KOH wet etch with existing silicon nitride mask on top as Figure 4b shows. The DRIE dry etch follows the remaining circular nitride hardmask pattern and creates circular shaped holes on the sidewalls of existing KOH etched holes. The combined wet and dry etches create holes with a combination of the square (on top) and circular shapes (at the bottom) as illustrated in Figure 4e. It can also be seen that there is a very abrupt change from 54.7° to 90° at the sidewall.

KOH wet etch and the combination of KOH and DRIE etches can create holes with tapered angles of 54.7°, neither of holes is deep enough to go through all the silicon intrinsic layer. Another simple dry etch method using reactive ion etch (RIE) is employed in this work, by controlling the resist etch profile, to achieve deeper etched holes with controllable sidewall angle. The detailed process of this method is presented in the Supporting Information S4. As shown in both Figure S4 and Table S2, the DUV resist at the holes spacing undergoes both sidewall profile and thickness changes as the RIE process continues, allowing some lateral etch at the opening of the holes, and finally resulting in the funnel-shaped holes with a depth of 3 μm as Figure 4c shows. The hole in Figure 4c has a sidewall angle of 61° at the opening and 83° at the bottom. By adjusting the initial DUV resist coating thickness and RIE process time, the etch holes can be achieved with desired depth and varying sidewall angle (between 61° and 83°) at the opening of the holes. It is able to use an empirical way to estimate the sidewall angle degree by examining the top view SEM images without cleaving the sample, and the details are presented in Supporting Information S6.

Dry etch can cause damages to the silicon surfaces due to the physical ion bombardment and these damaged surfaces can

DOI: 10.1021/acsphotonics.7b00486
ACS Photonics XXXX, XXX, XXX–XXX

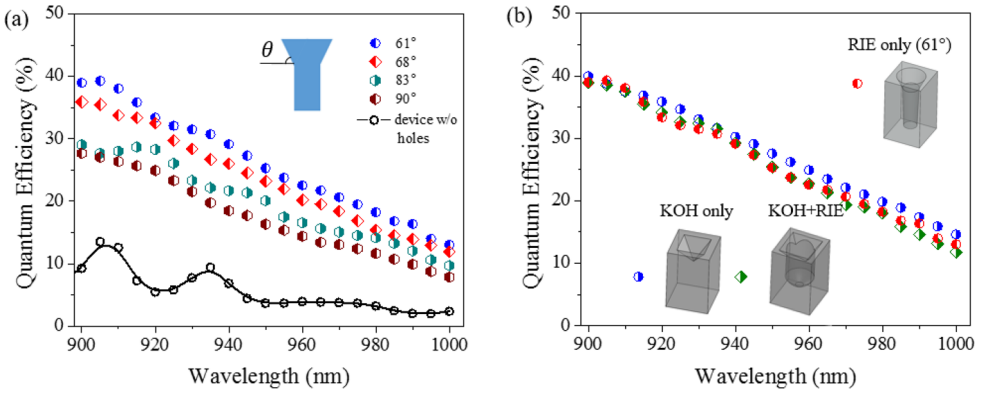

Figure 5. (a) Experimentally measured EQE of photodiodes with funneled submicron holes (d/p = 700/1000 nm, hexagonal lattice) of different angles and photodiodes without holes at wavelengths between 900 and 1000 nm: left-filled blue circles, 61°; left-filled red circles, 68°; right-filled green circles, 83°; left-filled brown circles, 90°; and ○ represent photodiodes without holes. (The inset shows the schematics of the funnel shaped holes with the angle of θ.) (b) Experimentally measured EQE of photodiodes with submicron holes (d/p = 700/1000 nm, hexagonal lattice) of different geometries etched by different fabrication techniques: left-filled red circles, funnel-shaped holes by RIE with sidewall angle of 61°; right-filled blue circles, inverted pyramids shaped holes by KOH wet etch; right-filled green triangles, integrated holes by combined KOH wet etch and DRIE dry etch. (The inset shows the 3D schematics of three types of the holes.)

serve as the defect sites and thus lead to undesirable surface states, traps and recombination sites[37,38] which would degrade the photodiodes' detection sensitivity and energy conversion efficiency. In this work, diluted hydrogen fluoride solution (HF/H_2O = 1:10) or silicon isotropic wet etchant ($HNO_3/H_2O/NH_4F$ mixed solution) is used for 10 s to remove DRIE and RIE associated surface damages of Si.[39] HF can provide hydrogen atoms to the dangling bonds at the Si surface and reduces these dangling bonds and metallic paths[40] and, hence, lowers the trapped charges at the surface. On the other hand, the silicon isotropic wet etchant can totally etch off these damaged silicon surfaces. Our results have shown that both methods are effective to passivate the dry etched silicon surfaces and minimize the leakage current of the photon-trapping holes based photodiodes by almost 2 orders of magnitude as shown in Figure S5 in the Supporting Information S7.

Factors Affecting the EQE of the Device. *1. Sidewall Angles.* Figure 5a shows the experimentally measured EQEs from photodiodes with holes (d/p = 700/1000 nm) in hexagonal lattice of different sidewall angles which are labeled with different colors. The holes with 90° angle are straight holes created by DRIE, while the RIE etched funneled holes with of 61°, 68°, and 83° were created via different DUV resist coating thickness and varying RIE time. The black circles in Figure 5a represent the measured EQEs of photodiodes without holes. The EQE measurements reveal that photodiodes with submicron holes outperform their counterparts without holes regardless of the sidewall angles. At the wavelength of 900 nm, the EQEs of the photodiodes with submicron holes are 28−40%, whereas the photodiode without micronanostructures is less than 10%. At another data communication wavelength of 980 nm, EQEs of the holes enabled photodiode are 10−20%, while the photodiode without micronanostructures only has less than 2%. This enhancement of absorption has also been seen in photonic crystal structures based solar cells.[19,21,25,41] In our case, the 10 times of EQE enhancement at the wavelength of 980 nm allows the operational wavelength of all-silicon photodiode extended to such wavelength close to the silicon's band edge. In addition, it also shows that the sidewall angles of the periodic submicron holes can greatly impact the EQE of the device: the smaller the sidewall angle, the higher EQE of the photodiodes. This is mainly because of the reduced reflection with funneled structure which can allow more coupling of light into the *i*-layer. The index difference at Si−air interface can be reduced by decreasing the amount of Si material in air matrix with those funnel shaped holes. The lower index change at Si−air interface can help light go through the medium instead of reflected back from the surface of the structure. The holes with 61° sidewall angle show the highest EQE over the spectrum that covers 900−1000 nm.

2. Different Geometries and Depths. As shown in Figure 4, three types of holes are created with different geometries and sidewall angles by KOH wet etch, the combination of KOH wet etch and DRIE and RIE, respectively. The 3D schematics of these holes are also illustrated in the inset of Figure 5 b. The same designs of the submicron holes (design (III): d/p = 700/1000 nm in a hexagonal lattice pattern) are used for comparison. It can be seen that the EQEs are very similar among the three types of holes between 900 and 1000 nm, with the KOH etched holes having slightly better performance. At the wavelength of 980 nm, the EQEs of holes from KOH etch, combined KOH/DRIE and RIE are 20, 18, and 18.5%, respectively. It should be noted that although the geometries are quite different among these holes, the sidewall angles of the holes are similar: both KOH and combined KOH/DRIE etched holes have a fixed angle of 54.7°, while RIE etched holes have a sidewall angle of 61° at the opening. The depths of the holes for design (III) are quite different among these geometries: RIE etched holes have the depth of more than 2.5 μm, KOH etched holes only have depths of 500−600 nm, and combined KOH/DRIE etched holes can reach to 800−900 nm. This indicates that, as long as the lateral propagating modes can be generated by the periodic holes, the depths of the holes do not seem to affect the EQEs as much as the sidewall angles do. The slightly lower EQE of KOH/DRIE etched holes may be caused by the abrupt angle change on the sidewalls of the holes, which may lead to a slightly different reflection from the surface.

3. Dimensions and Lattice Patterns. Total of 12 cases, including 6 designs in hexagonal and square lattice, are compared at different wavelengths between 850 and 980 nm: (I) d/p = 1300/2000 nm, (II) d/p = 1500/2000 nm, (III) d/p

DOI: 10.1021/acsphotonics.7b00486
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= 700/1000 nm, (IV) d/p = 630/900 nm, (V) d/p = 1500/2500 nm, (VI) d/p = 1300/2300 nm. The lattice parameter effect on the resonant modes has also been observed in ref 42. In our case, as shown in the Supporting Information S8, the holes in hexagonal lattice pattern have better EQE of the holes in square lattice pattern of the same design. This trend is more obvious at the 850 nm compared to 980 nm.

On the other hand, as shown in Figure S6 in the Supporting Information S8, smaller hole designs III (d/p = 700/1000 nm) and IV (d/p = 630/900 nm) in hexagonal have the highest EQEs among all the designs. Similar observations are also noticed in KOH etched and combined KOH/DRIE holes. This indicates that the light incident on the photodiodes with holes of smaller dimension designs can be more easily trapped and generate the lateral modes to enhance the absorption in the active region at those wavelengths.

When the diameter of the holes is a constant, the period between the two holes is also a factor to consider to achieve the optimal EQEs. In our designs, there is a trend that smaller period generally leads to a slightly better EQE performance of the photodiodes. For hole diameters of 1300 and 1500 nm, designs of I and II with smaller period, outperform designs of VI and V with larger period, respectively. However, the design of the period has to be practical, taking into account of the fabrication variation to avoid the interconnection of adjacent holes.

Responsivity and High Speed. The device responsivity can be calculated using $R = \eta \times \frac{\lambda}{1.24}$ (A/W), where R is responsivity, η is external quantum efficiency, and λ is the wavelength in μm.

The device responsivities of different holes between 900 and 1000 nm are shown in Figure 6. It can be shown that the inverted holes etched by KOH have the best performance between 900 and 1000 nm among all the holes with the same design (III) with d/p = 700/1000 nm, in a hexagonal pattern. At the wavelengths of 980 and 1000 nm, the responsivities of the device with KOH etched holes are around 0.16 and 0.12 A/W, respectively. They are almost 10-fold of the responsivities of the device without photon-trapping holes. The device responsivity values (measured at 850, 880, 910, and 940 nm) are sufficient to meet the power budget requirements of current SWDM systems.[3] The device can also be used in future SWDM systems using 980 nm as well as HPC and LIDAR systems.

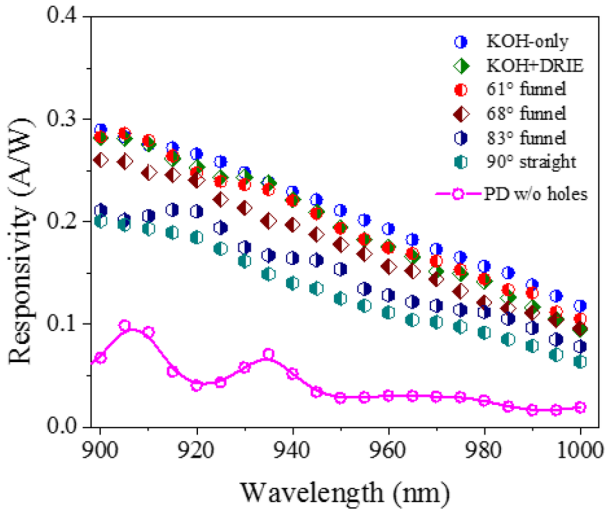

Figure 6. Experimentally measured responsivities of photodiodes based on different holes including KOH etched only, KOH/DRIE combination, RIE etched funneled holes with side wall angle of 61°, 68°, and 83°, and straight holes etched by DRIE, compared to photodiodes without any submicron holes between 900 and 1000 nm. The holes' design is (III), with d/p = 700/1000 nm in a hexagonal pattern.

Figure 7 shows the photoresponse of a 30 μm photodiode with photon-trapping holes in the form of electrical pulses observed on a 20 GHz oscilloscope. The full-width half-maximum (fwhm) value of the temporal responses above 3 V reverse bias at the wavelengths of 900 and 980 nm are measured to be 30.3 and 30.7 ps, respectively. It should be noted that the peaks of the pulse amplitude are different at these wavelengths, and this is related to the different EQEs at such wavelengths. The temporal responses at other wavelengths are summarized in Table 1. The fast response of the device is capable of supporting both 10G and 25G operations at these wavelengths.

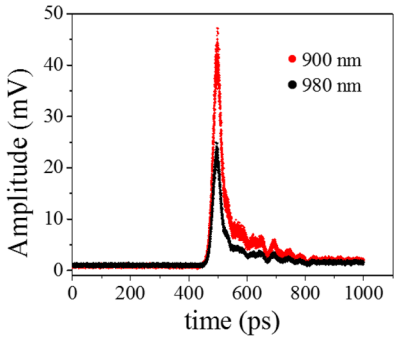

Figure 7. High-speed responses of a 30 μm photodiode with photon-trapping holes at the wavelength of 900 nm (red) and 980 nm (black), showing the temporal pulse with fwhm value of 30.3 ps (900 nm) and 30.7 ps (980 nm).

Table 1. Temporal Responses of a 30 μm Silicon Photodiode with Photon-Trapping Holes at the Wavelengths between 900 and 1000 nm

wavelengths (nm)	fwhm (ps)
900	30.3
950	31.1
980	30.7
990	32.7
1000	34.3

CONCLUSION

This study demonstrates the design and fabrication of an all-silicon photodiode with photon-trapping submicron holes structures. These photon-trapping holes successfully enhance the absorption of Si and extend the operational wavelength of the photodiode to 1000 nm with an external quantum efficiency of 20% and responsivity of 0.16 A/W. This represents more than 10-fold increased efficiency compared to Si devices without any photon-trapping holes. The thin intrinsic layer allows this photodiode to be able to operate at ultrahigh speed with a temporal response of ~30 ps at 900 and 980 nm. Multiple parameters of the submicron holes including dimensions, sidewall angles, lattice patterns, and different etch

DOI: 10.1021/acsphotonics.7b00486
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methods affect the absorption in silicon and, thus, lead to considerably different external quantum efficiencies in different photodiodes with different types of holes. We experimentally observed that, among many different designs, photodiodes with periodic funneled holes of 700 nm in diameter and 1000 nm in period, etched via the RIE process, with 61° sidewall angle, and in a hexagonal lattice exhibit the optimal quantum efficiency, as high as 40% at 900 nm. While with the same hole design, an inverted pyramid hole based device etched by KOH exhibits the best quantum efficiency of more than 20% at 980 nm. The devices also show broadband absorption characteristics with high quantum efficiencies between 900 and 1000 nm, which covers all the wavelengths of short wavelength division multiplexing and part of the wavelengths used in high performance computing systems and LIDAR systems. Most importantly, our all-silicon photodiode is fabricated using CMOS compatible processes.

METHODS

Fabrication of Photon-Trapping Holes Based All-Silicon Photodiode. All the fabrication processes for the photodiodes are CMOS compatible and were done in a class 100 clean room. Briefly, the PIN SOI wafer was precleaned in piranha solution to remove any organic residue. 100 nm of PECVD silicon nitride film was coated on the wafer at 250 °C for KOH etched holes (DRIE and RIE holes are fabricated without the PECVD nitride film). Then, DUV lithography was used to pattern the submicron holes, and then DRIE and RIE were employed to create straight and funneled shape submicron holes, respectively. For KOH etched holes, DRIE was used to pattern the nitride hardmask, and then the wafer was immersed in 24% KOH solution for 2 min at 65 °C. Next, DRIE was used to etch the *n*-mesa to *p*-Si layer and *p*-mesa to the SOI substrate. *N*-ohmic and *p*-ohmic metal rings that consist of 100 nm of Al and 20 nm of Pt are deposited on *n*-mesa and *p*-mesa, respectively, by evaporation followed by a lift off process. To minimize the leakage current, the wafer was treated in HF or silicon isotropic etchant for 10 s. Finally, the whole device was passivated with an insulating layer consist of 150/300/150 nm $Si_3N_4/SiO_2/Si_3N_4$ thin layers with contact open. The alternate nitride and oxide layers are used to minimize the effect of possible pinholes and maximize the insulating effect.[43]

External Quantum Efficiency (EQE) Measurement Setup. EQE of a photodiode is defined as number of excess electrons per number of incident photons. This definition can be rewritten as following equation:

$$\mathrm{EQE} = \frac{I_{\mathrm{ph}}/e}{P_{\mathrm{in}}/h\varpi}$$

where EQE is the external quantum efficiency, I_{ph} is photocurrent, e is one electron charge, P_{in} is the incident optical power, and $h\varpi$ is the energy of a single photon. A supercontinuum laser and a tunable filter that transmits a band of wavelengths with 5 nm width was used to conduct EQE measurements. The light is delivered to the devices by a single-mode fiber probe on a probe station.

High-Speed Measurement Setup. A supercontinuum tunable laser source with mode-locking technology has been used to conduct high speed measurements in the wavelength range of 900−1000 nm. The pulse width is sub picosecond (ps) and the repetition rate is 80 MHz. The pulse spectral width is 1−5 nm with a total output average power of 40 μW. A device with a diameter of 30 μm is tested with a ground-signal-ground (GSG) microwave probe on a microwave probe station. The light was focused onto the active region of the photodiodes using a single-mode lensed fiber tip and was aligned with a translational stage to maximize the photocurrent.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsphotonics.7b00486.

Simulated external quantum efficiency (EQE) of photodiodes with funneled holes of different sidewall angles at the opening; Creating straight submicron holes; Isotropic wet etch and dry etch to create shallow tapered holes; KOH wet etch to create inverted pyramid-shaped holes; RIE to create funnel-shaped holes with varying sidewall angles; Estimation of the sidewall angle of RIE etched holes via top view SEM image; Dimension and lattice pattern effect on the EQE at wavelengths of 850 and 980 nm (PDF).

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Author Contributions

E.P.D., A.F.E., and S.G. did the simulation. M.S.I., Y.G., H.C., and S.-Y.W. designed the photodiodes. Y.G. and H.C. fabricated the devices. H.C., C.B.P., S.G., and Y.G. carried out the EQE and high-speed characterization of the photodiodes. Y.G., H.C., S.G., A.F.E., and T.Y. discussed the processing and characterization results and analyzed the data. Y.G. drafted the manuscript. S.-Y.W., T.Y., E.P.D., A.F.E., and M.S.I. revised the manuscript. S.-Y.W. and M.S.I. cosupervised this project. All authors have given approval for the final version of the manuscript.

Notes

The authors declare no competing financial interest.

ACKNOWLEDGMENTS

We thank S. P. Wang and S. Y. Wang Partnership for financial support. Partial support from ARO (W911NF-14-4-0341) is gratefully acknowledged. We also thank Lawrence Semiconductor Research Laboratories (LSRL) for supplying us epi growth wafers and providing spreading resistance profiles.

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DOI: 10.1021/acsphotonics.7b00486
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DOI: 10.1021/acsphotonics.7b00486
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A High Speed Surface Illuminated Si Photodiode Using Microstructured Holes for Absorption Enhancements at 900−1000 nm wavelength

Supporting Information

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S1. Simulated external quantum efficiency (EQE) of photodiodes with funneled holes of different sidewall angles at the opening.

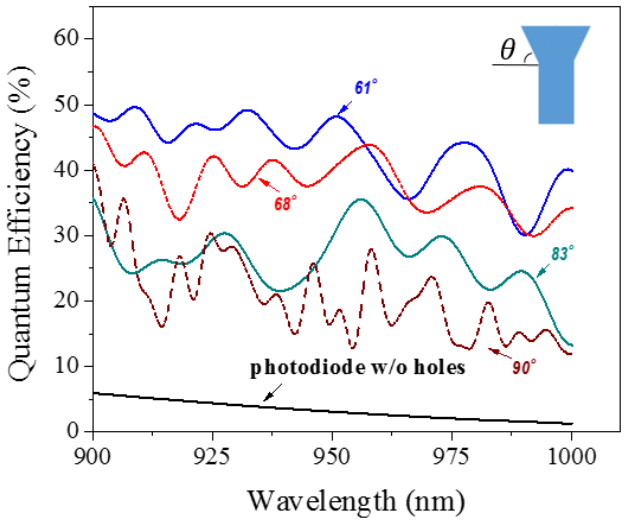

Figure S1. Simulated EQE of photodiodes with funneled submicron holes (diameter: 700 nm, period: 1000 nm, in hexagonal lattice pattern) of different angles and photodiodes without photon-trapping holes at wavelengths between 900-1000 nm. Blue: 61º, Red: 68º, Green: 83º, Wine: 90º; Black lines shows the photodiode without holes. The simulated absorption i-layer thickness is 2 μm. Inset shows the schematic of the funneled holes with a sidewall angle of θ at the opening.

It is evident from Figure S1 that the simulated EQE values agree with the experimental data trend for all angles in Figure 5(a). The discrepancies between the simulation and measured EQE are likely to be caused by the fabrication process induced variations of dimensions, surface defects, and the reduced i-layer thickness by the heavily doped dopant diffusion from n+ and p+ layers compared to the designed value used in the simulation. It should be noted that the resonant peaks in the simulation become less obvious in the measured data. The simulation assumes vertical light incident into the photodiode, however, in reality, the laser light from the fiber probe is not perfectly vertical and may come at several angles into the holes, and this may lead to the disappearance of the resonant peaks at a number of wavelengths.

S2. Creating straight submicron holes

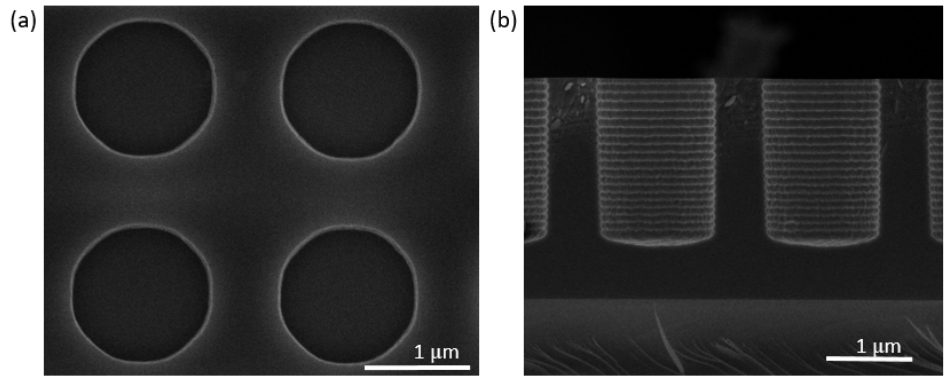

Figure S2. (a) Top view SEM of straight holes by DRIE; (b) Cross-sectional SEM of straight holes by DRIE. The holes are 1300 nm in diameter and 2000 nm in period (d/p=1300/2000 nm) and are in square lattice in both (a) and (b).

Bosch process is commonly used to create very high aspect ratio straight holes, especially in Micro-Electro-Mechanical Systems (MEMS) applications.[1] In this work, Bosch process which consists of alternative passivation and etch steps is used to create the straight submicron holes in the DRIE etching system. In the passivation step, 100 sccm of C_4F_8 is introduced into the etcher chamber to passivate all surfaces for 3 s. In the etch step, 130 sccm of SF_6 and 13 sccm of O_2 are introduced into the etcher chamber to etch Si anisotropically for 3.5 s. Then, the passivation and etch cycles repeat when the desired depth of the submicron holes is reached. This process has a very high selectivity of Si to deep ultraviolet (DUV) resist up to 50:1, and it allows high aspect ratio etch. The top view and cross-sectional SEM images of the straight submicron holes in our photodiodes are shown in Figure S2 (a) and (b), respectively.

S3. Isotropic wet etch and dry etch to create shallow tapered holes

Silicon isotropic wet etchant is made from a mixed solution of HNO_3/ H_2O/ NH_4F (64:33:3).[2] This etchant can also etch PECVD deposited Si_3N_4 hardmask as well, but with a slower etch rate compared to silicon. As Figure S3(a) shows, the Si_3N_4 hardmask was eroded and the hardmask

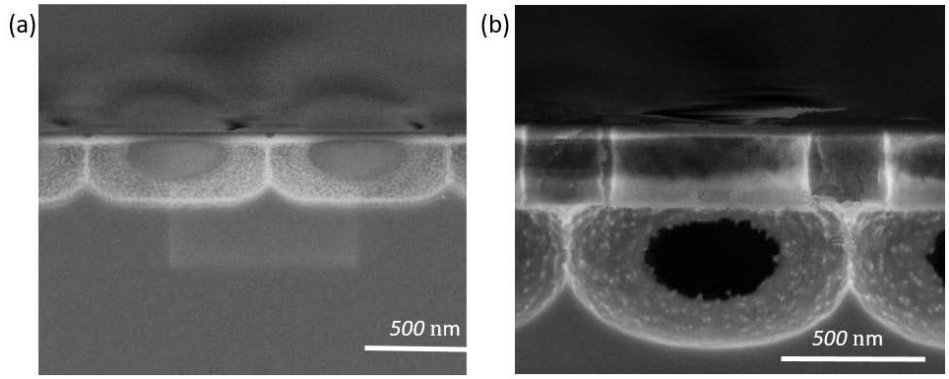

Figure S3. (a) Cross-sectional SEM image of tapered holes by silicon isotropic wet etch (HNO_3:H_2O:NH_4F) solution. The submicron holes are interconnecting (d/p=630/900 nm); (b) Cross-sectional SEM image of tapered holes by DRIE isotropic dry etch (SF_6 gas). The submicron holes are interconnecting (d/p=700/1000 nm). Note that hardmasks are present in all images [40 nm Si_3N_4 hardmask in (a) and 300 nm DUV resist mask in (b)]

pattern was enlarged during the 2 min etch (hole pattern diameter before the silicon isotropic wet etch: 630 nm, hole dimension after wet etch: 825 nm). The enlarged hardmask pattern together with the isotropic nature of this etchant results in interconnecting holes with a depth of only 285 nm. SF_6 gas in the DRIE process is also used without the C_4F_8 passivation step for the isotropic dry etch. Similarly to the isotropic wet etch, the nature of the pure SF_6 gas results in almost identical lateral etch rate as vertical etch rate and thus producing large undercut beneath the photoresist as Figure S3(b) shows. However, the selectivity of Si to DUV resist is much better in SF_6 based isotropic dry etch, and the lateral erosion of the resist hardmask is minimal, resulting in deeper holes of 500 nm compared to isotropic wet etch. The resulting etched holes by the isotropic dry etch also have similar interconnecting issues as the dry etch continues.

S4. KOH wet etch to create inverted pyramid-shaped holes

350 nm thick PECVD silicon nitride film is used as a hardmask for KOH wet etch. KOH (24 wt. %) wet etch is conducted at 65℃, and the intersection of the (1 1 1) planes causes self-limiting

etch after around 2 minutes and forms inverted pyramid shaped holes. The depths and widths of the KOH wet etched holes are dependent on the diameters of the holes as Table S1 shows.

Table S1. Summary of the depths of KOH wet etched holes.

Type	Designed diameter/ period (nm)	Depth (nm)	Width at the opening (nm)
I	1300/2000	1000	1520
II	1500/2000	1210	1710
III	700/1000	605	870
IV	630/1000	540	740

S5. RIE to create funnel-shaped holes with varying sidewall angles

As shown in Figure S4(a), the sidewall of the deep ultraviolet (DUV) resist (represented in blue color) is almost vertical before the RIE process. Due to the high density of the submicron holes in our PDs and the lateral etch of the resist, the resist between the submicron holes starts to form a positive angle after 10 min of RIE process as indicated in Figure S4 (b). At this stage, the height of the resist between the submicron holes (the height of blue triangle in Figure S4 (b)) is the same as the measured thickness of the bulk resist which is on some large features without submicron holes (both are around 850 nm). As the etch process continues, the tapered profile of the resist in the submicron holes' region is subject to faster etch rate, and further decreases the angle of the resist. When the thickness of the resist between the spacing of the submicron holes continues to decrease, the submicron holes start widening, creating tapered angles. However, this lateral etch is only affecting the opening of the holes, while the angle of the submicron holes at the bottom remains around 83º. Figure S4 (e) shows the top view SEM image of the submicron holes of Figure S4 (d) after the resist is stripped. The black rings inside the submicron holes

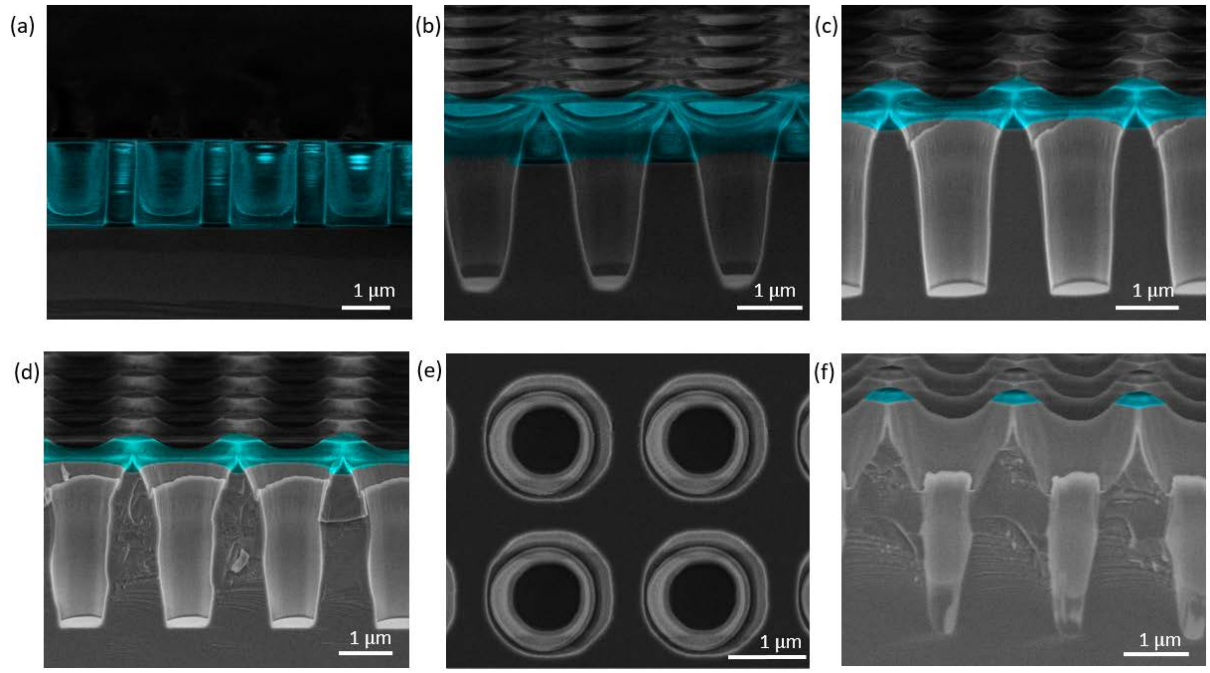

Figure S4. (a) Cross-sectional SEM image of patterned DUV resist of 1.7 µm thick (blue color) on Si surface; (b) Cross-sectional SEM of DUV resist and holes after 10 min RIE process, the angle of the holes is around 82º; (c) Cross-sectional SEM image of DUV resist and holes after 13.8 min RIE process with 500 nm measured bulk resist thickness (not shown here), the angle of the holes is around 71º; (d) Cross-sectional SEM image of DUV resist and nanoholes after 14.9 min RIE process with 400 nm measured bulk resist thickness (not shown here), the angle of the holes is around 65º; (e) Top view SEM image of holes in (d) after stripping the DUV resist; (f) Cross-sectional SEM image of DUV resist and holes after 18 min RIE process with 160 nm measured bulk resist thickness (not shown here), the holes are interconnecting with each other at the opening. (The design of the holes are 1300 nm in diameter and 2000 nm in period (d/p=1300/2000 nm) and are in square lattice in (a)-(f). For better perception, the resist is colored only at cross-section sites)

correspond to the nanotrenching at the intersection of the sidewalls of two different angles. The nanotrenching is caused by the Cl_2 ions reflection from the sidewall.[3-4] Compared to straight holes, the nanotrenching phenomenon is more severe in our case, since our process made the sidewall more tapered allowing Cl_2 ions to reflect at a larger angle. As the RIE process continues, the resist in the spacing of the holes is etched away, and the submicron holes start to interconnect with each other as shown in Figure S4(f). However, at this stage, this is still around 160 nm of bulk resist left. We would like to avoid the cases that interconnect the holes, since intercepting holes overetch the top *n*-layer and may cause contact issues and lower the EQEs of

the devices. Table S2 shows the summary of the thickness of the bulk resist, resist in the spacing and corresponding submicron holes angles. We also show a convenient way to estimate the sidewall angle of the holes by examining the top view SEM image.

Table S2. Summary of the thickness of bulk resist, resist in the spacing of the holes and corresponding angles of holes at different stages of the RIE process.

Etch time (min)	Bulk resist thickness (nm)	Resist thickness in the spacing (nm)	Angle of the holes at the opening (º)
10	845	840	82
13.8	500	260	71
14.9	400	200	65
18	160	0	Intercepting holes

S6. Estimation of the sidewall angle of RIE etched holes via top view SEM image

In this work, we are interested in sidewall angle of the holes between 60-90º. We noticed that the nanotreching locations are rather similar among holes with different designs: around 0.4-0.45 μm deep from the Si surface. In this case, since it is not practical to break all the wafers in different conditions to measure the sidewall angle, it is a convenient way to estimate the angle of the holes (θ) using following formula with the information from the top view SEM images of the holes in Figure S4(e):

$$\theta = \arctan\left(\frac{d_{outer} - d_{inner}}{2 \times 400}\right) \quad (1)$$

Where d_{outer} is the outer diameter of the holes (nm);

d_{inner} is the inner diameter of the holes (nm), i.e. the diameter of the black ring in the SEM;

400 is the depth of the nanotreching (nm).

S7. Passivation of the dry etch induced silicon damaged surfaces

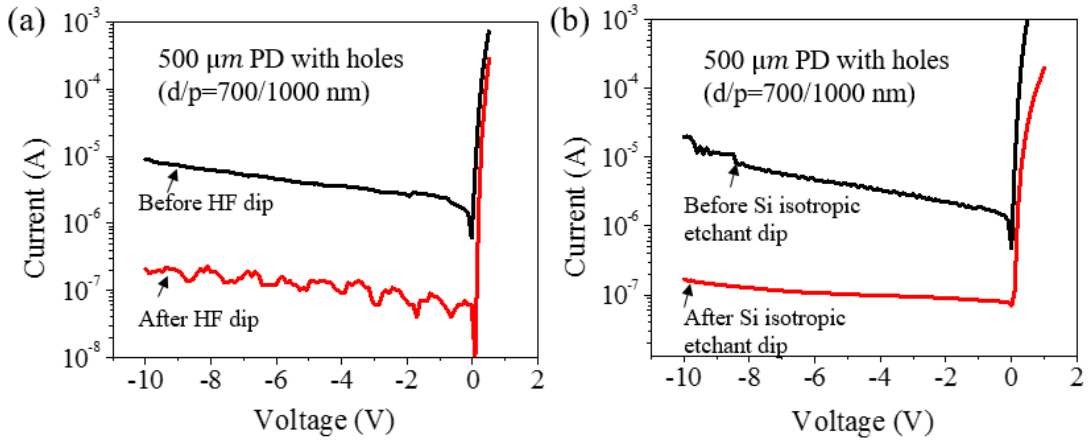

Figure S5. Leakage current of a 500 μ*m* PD with holes (d/p=700/1000 nm) (a) before and after HF dip; (b) before and after Si isotropic etchant dip.

S8. Dimension and lattice pattern effect on the EQE at wavelengths of 850 and 980 nm.

Figure S6 show the experimentally EQE of photodiodes of funneled holes (61º angle) and straight holes (90º angle) in both square and hexagonal lattice with different hole diameters (d)

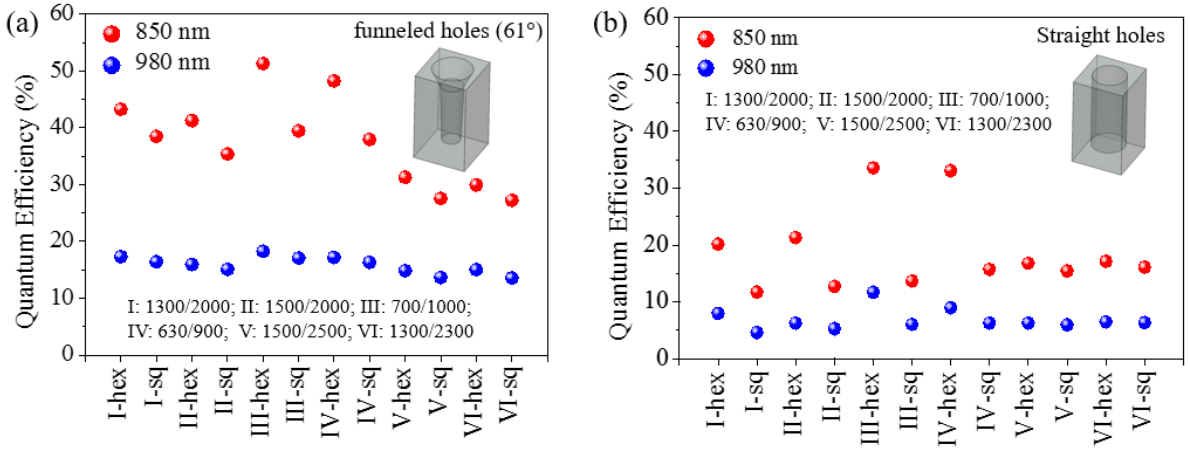

Figure S6. Experimentally measured EQEs of photodiodes based on different designs of (a) funneled holes with side wall angle of 61º and (b) straight holes at wavelengths of 850 and 980 nm. Design I represents holes with d/p=1300/2000 nm; II: 1500/2000 nm; III: 700/1000 nm, IV: 630/900 nm, V: 1500/2500 nm, VI: 1300/2300 nm. "hex" represents holes in hexagonal lattice, while "sq" is in square lattice. The insets are showing the schematics of funneled and straight holes.

and periods (p) at wavelengths of 850 and 980 nm. At 850 nm, especially for designs I, II, III, and IV, the holes in hexagonal pattern have considerably higher EQE than the ones in square lattice pattern. For example, for design III (d/p=700/1000 nm), the EQE of funneled holes in hexagonal lattice is 52%, while EQE of the funneled holes in square lattice is 40%. The lattice pattern effect is more obvious for straight holes: for the same design III, the EQE of straight holes in hexagonal is 34%, while the ones in square lattice is 16%, over 100% increase. However, at the wavelength of 980 nm, the lattice pattern effect is not as same obvious, with holes in hexagonal lattice only outperform the ones in square lattice by less than 10%.

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