High-Speed High-Efficiency Broadband Silicon Photodiodes for Short-Reach Optical Interconnects in Data Centers

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Abstract: We demonstrate a silicon-based surface-illuminated CMOS-compatible broadband photodiode with ≤30ps FWHM and above 55% EQE at 850nm for up to 50Gb/s by using photon-trapping micro/nano-structures. This is the fastest reported response for a Silicon photodiode.

OCIS codes: (230.5170) Photodiodes; 040.5160 Photodetectors; 230.5298 Photonic Crystals

1. Introduction:

Application of Silicon photodiodes (SiPD) in the new short wavelength division multiplexing (SWDM) that is being proposed for data center communication is hindered by low quantum efficiency in the range of 850-950 nm due to the small absorption coefficient (α) close to silicon band gap (1.12 ev) [1, 2]. Designing a high-speed and high-efficient SiPD has been challenging as an efficient Si-based photodiode (PD) requires a thick intrinsic (i)-layer, which increases the transit time of the photo-generated carriers. Commercially available SiPDs are limited to data communication rate of 2Gb/s or less due to long transit time of photo-generated carriers in the thick absorbing region (i.e. 10 μm).

A CMOS-compatible surface-illuminated SiPD with photon-trapping micro-/nanostructures [3, 4], providing >50% quantum efficiency (EQE) and <30ps full-width at half-maximum (FWHM) impulse response at 850 nm has been recently demonstrated using nip structure. Both low speed and low external quantum efficiency (EQE) challenges are addressed by designing PDs with thin absorption region integrated with periodic arrays of micro-/nano holes that can redirect the Poynting vector of a surface incident optical wave to propagate parallel to the PD surface to facilitate efficient photon absorption. In this paper, a similar SiPD with pin structure and improved performances (29ps FWHM) and a deconvolved response of 22ps is reported. A PD model including carrier transport and PD equivalent circuit is developed. Also simulated eye-diagrams at 25 and 50Gb/s are presented and discussed. The results show that highly efficient SiPDs are capable of operating at 25 Gb/s data rate and have potential to reach to 50Gb/s with an equalizer.

2. Device Design and Fabrication:

The PD structure was epitaxially grown on a silicon-on-insulator (SOI) substrate that includes a 0.2 μm device layer (p-Si). In order to minimize the transient time of photo-generated electron-holes, a thin (2μm with background doping of mid E16 1/cm^3) absorbing medium (i-Si) is sandwiched between a lattice-matched 0.2μm heavily doped p-Si (top contact) and an n-Si (bottom contact) 0.3μm layers. The devices have mesa structures with pin on a SOI wafer with a 3 μm buried SiO_2 layer (Fig. 1a).

Fig.1 a) Proposed SiPD structure integrated with nanohole surface structure, b) Fabricated 30μm diameter SiPD on SOI (Silicon-on-Insulator) wafer used for EQE and high-speed measurement.

In order to overcome the weak photon absorption in PDs, an array of 2D periodic micro/nano holes are integrated in the thin absorbing region. To reach the optimum structure which offers the highest optical absorption in nanohole structures, various diameter/period (1300/2000nm and 700/900nm) and nanohole arrangement (Hexagonal and

square) were etched to the depth of the bottom player (Fig. 1b). Details of PD fabrication process were similar to the nip structures that discussed in Ref. [3, 4].

3. Experimental Results:

The devices with lateral propagating modes experience enhanced photon-matter interactions and resulted in measured maximum EQE of 37% for cylindrical holes (Fig. 2a, blue color) and more than 55% EQE for funnel shape holes (Fig. 2a, navy and green color) at 850nm wavelength. Measured EQE represents an enhanced absorption coefficient ($\alpha_{eff.}$) of approximately 10 times (850nm) higher than bulk Si (Fig. 2b). It implies that one needs more than 13 times thicker i-Si layer to achieve the same amount of absorption in silicon film without micro/nano holes. Based on doping profile, i-layer thickness was estimated to be 1µm. Higher EQE around 65% is expected for future devices with funnel shape micro/nano holes and 2µm thick absorbing region.

Fig.2 : a) Measured EQE Vs. wavelengths in SiPDs with micro/nano holes, b) Absorption coefficient in SiPD, bulk Si, and GaAs.

To conduct high-speed measurements, a mode-locked sub-picosecond pulsed laser (λ=850nm) with repetition rate of 20 MHz was used on a microwave probe station. A 30µm diameter device was tested with a microwave probe (GSG) and the light beam was aligned with a translational stage to maximize the photocurrent. The impulse response FWHM of SiPD with -3v, -10v, and -15v bias is measured to be 34ps, 31ps, and 29ps respectively. The long tail observed after signal fall time is caused by slower diffused carriers generated in the dopant diffusion regions at p-i and i-n interfaces. It has demonstrated in figure 3a that the difference in FWHM of impulse response at different applied biases is not as drastic as the change in tail suppression with larger bias. The doping concentration of i-layer in Si PDs utilized in this study requires to bias the PDs at high voltage to deplete at least 1µm. The variable depletion region with bias causes voltage-dependent capacitance and hence voltage-dependent impulse response.

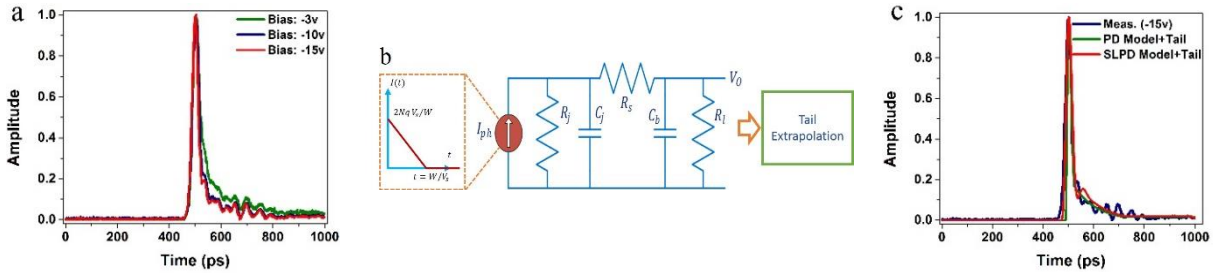

Fig.3: (a) Measured impulse response by applying different reverse voltage bias (green: -3v, navy: -10v, and red: -15v); (b) PD model block diagram which consists of electron-hole generation in active region through photon absorption mechanism and PD equivalent circuit, and the tail added to the model through extrapolation process using measured curves; (c) Compares the measurement result (-15v) (navy, FWHM=29ps), PD model with tail extrapolation (green, FWHM=22ps), and PD model with extrapolation after considering sampling oscilloscope and laser pulse width effects (red, FWHM=29ps).

We have modeled our PD with a current source (Iph) with triangular waveform due to incident light impulse. This current source represents the uniform electron-hole generation inside the i-layer with thickness W. The equivalent PD circuit includes large shunt resistance (Rj), junction capacitance (Cj), series resistance (Rs), bonding capacitance (C_b), and load resistance (R_l). Circuit components are obtained via device I-V (forward bias) and C-V measurements and R_l assumed to be 50Ω. Using measured data, an extrapolated tail is added to PD model to make the model close to realize the impulse response (fig. 3b). Considering the effect of 20GHz sampling oscilloscope and optical pulsed laser in the measurement, the Scope-Laser-PD Model (SLPD) has shown agreement with measurements (Fig. 3c, red color). The simulation results also indicate that the device impulse response FWHM to be 22ps (Fig. 3c, green color). This is the fastest reported response for a Si photodiode with such wide-spectral high EQE.

We evaluated the performance of SiPD for transmission speed using computer simulation. A pattern of 2000 random bits has been simulated (similar to IEEE 802.3bm) and convolved with the PD impulse responses under different bias.

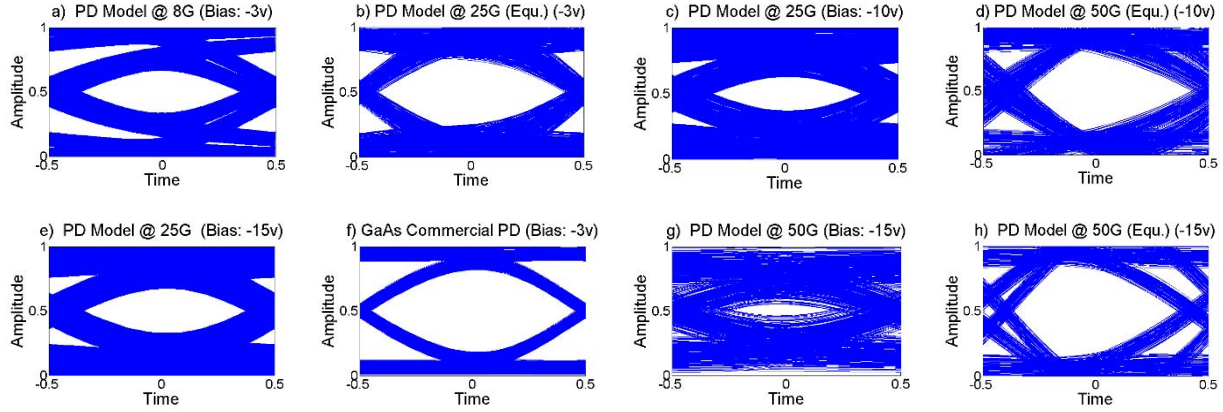

Fig.4: SiPD performance at a) 8Gb/s (Bias:-3v), b) 25Gb/s with equalizer (Bias:-3v), c) 25Gb/s (Bias:-10v), d) 50Gb/s with equalizer (Bias:-10v), e) 25Gb/s (Bias:-15v), f) Commercial GaAs PD performance at 25Gb/s (Bias:-3v), SiPD performance at g) 50Gb/s (Bias:-15v), h) 50Gb/s with equalizer (Bias:-3v)

To simulate the effects of trans-impedance amplifier (TIA), the PD output is applied to a third order Butterworth filter with 3-dB bandwidth equal to 0.75*Bit Rate [5, 6]. The simulated eye diagrams at the filter output with -3v bias have shown in Figures 4a and 4b for 8Gb/s and 25Gb/s, respectively. The results indicate possible operation at 8Gb/s without equalization and 25Gb/s using a simple two tap Feed Forward Equalizer that is proposed in [7]. Device impulse response with -10v bias was used in simulation to generate eye diagram in figure 4c and 4.d. It has shown the fabricated SiPD potential to operate at 25Gb/s bit rate without equalizer. Moreover, using the equalizer SiPD is capable to perform at 50Gb/s properly. It has demonstrated that applying higher reverse bias can suppress the added long tail to the impulse response which leads to improve the SiPD performance at higher bit rates. In order to reach the supreme device performance, we increased the device bias to -15v. Compared to -10v biased results (Fig. 4c), simulated eye diagram (Fig. 4e) has illustrated that SiPD performance with -15v bias is more reliable at 25Gb/s. To validate the results, we compared the SiPD performance at 25Gb/s with a commercially available GaAs photodiode. The GaAs PD high-speed measurement was conducted using the same setup (Fig. 4f). Although GaAs commercial PD was shown a superior performance at 25Gb/s compared to proposed SiPD, it can be found that the SiPD performance at such high-speed bit rate is promising. SiPD operation at higher rates has demonstrated that the integration of reported SiPD with equalizer could be operational at 50Gb/s (Fig. 4g and 4h).

4. Conclusion:

A CMOS-compatible SiPD with observed quantum efficiency (>55% EQE for 840nm-860nm) that is capable to operate up to 50Gb/s data communication rates is demonstrated. The efficient high-speed SiPDs are suitable for monolithic integration with CMOS electronics to reduce the cost of optical transceivers used for short-reach multimode optical data links in datacom and computer networks.

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