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A novel interconnection technique for manufacturing nanowire devices

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ABSTRACT This paper reviews a novel bridging technique that connects a large number of highly directional metal-catalyzed nanowires between pre-fabricated electrodes and extends the technique to an electrically isolated structure that allows conduction through the nanowires to be measured. Two opposing vertical and electrically isolated semiconductor surfaces are fabricated using coarse optical lithography, along with wet and dry etching. Lateral nanowires are then grown from one surface by metal-catalyst-assisted chemical vapor deposition; nanowires connect to the other vertical surface during growth, forming mechanically robust 'nanobridges'. By forming the structure on a silicon-on-insulator substrate, electrical isolation is achieved. Electrical measurements indicate that dopant added during nanowire growth is electrically active and of the same magnitude as in planar epitaxial layers.

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1 Introduction

Technological limitations and escalating costs of increasing electronic device density by the 'top-down' approach have generated interest in alternatives to enhance the functionality of conventional electronics. Significant progress has been made in the area of 'bottom-up' technology, in which functional nanostructures are assembled from chemically synthesized, nanoscale building blocks. One-dimensional (1D) nanowires of various materials have been synthesized with controlled and tunable chemical composition, structure, size, morphology, and electrical properties [1–7]. Researchers have demonstrated a number of functional nanowire devices, such as nanoscale field-effect transistors (FETs) [3, 8], *p–n* junction diodes [3], light-emitting diodes (LEDs) [3], bipolar junction transistors [3], complementary inverters [3], logic gates [1], and lasers [9]. Semiconductor nanowire sensors show promise for extremely sensitive, direct (bio)chemical-to-electrical transduction and, with proper functionalization, should also have excellent selectivity [10–15]. New applications and novel device concepts may emerge from quantum effects arising from the small diameters of the nanowires [16].

Synthesis of 1D semiconductor structures was first reported by Wagner and Ellis in 1964, when they demonstrated micrometer-diameter, 1D structures [17]. The field of semiconductor nanowire synthesis was pioneered by Hiruma and coworkers at Hitachi Labs [1]. Their approach was further developed by several groups to explore 1D nanostructure growth and applications to nanoelectronic and photonic devices [3–5, 18–20]. Selected electrical, optical, mechanical, and thermal properties of such nanostructures have been predicted to be superior to the properties of conventional electronic and photonic devices [15, 21–26].

A significant roadblock to wide-scale integration of functional nanowire devices is the difficulty in connecting nanowires to microscale electrodes. An optimum technique for integrating nanowires with conventional electronics should be widely applicable, compatible with current integrated-circuit (IC) processing methods, and cost effective. In addition, precise control of the nanowire length, density per unit area, contact resistance, and mechanical robustness is highly desirable. Previously reported techniques for interfacing nanowires fail to meet all of these requirements, and a new approach is needed for integrating nanowires with conventional circuitry.

In many previous demonstrations, connecting metal-catalyzed nanowires to electrodes required complex additional processing. For example, the nanowires were often detached from the substrate on which they were grown and placed into solution [3]. The liquid dispersion was then forced to flow through channels defined in the receiving substrate, leaving some nanowires on the substrate. Electrodes were then deposited to make connection to the nanowires remaining in the channels. These extra steps complicate the overall device fabrication. In other cases, electrical contacts were defined with electron-beam lithography on a few selected nanowires [25]. Although connecting electrodes to nanowires one at a time enables studies of the characteristics of the nanowires and the exploration of novel device applications, it cannot be used for reproducible mass fabrication of dense, low-cost device arrays. A massively parallel technique is needed to allow self-assembly of nanowires between electrodes using only relatively coarse lithography.

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We have developed a technique for growing nanowires and forming the connections during nanowire growth [6]. This technique is suitable for mass production and can be made compatible with existing microelectronics fabrication processes. It combines the 'bottom-up' fabrication of nanostructures with the 'top-down' formation of the connecting electrodes to form nanodevices using only low-cost optical lithography. In an initial investigation, we demonstrated the concept of connecting the nanowires ('bridging') during the growth process on a bulk (110)-oriented wafer [6]. In this paper, we review the basic concept and initial demonstration and extend the technique to the electrically isolated structure needed for devices.

2 Synthesis of nanowires between electrodes: concept

Nanowires are often synthesized by 'metal-catalyzed' chemical vapor deposition [2, 5, 27]. This technique results in nanowires with small diameters without using fine-scale lithography. To grow silicon nanowires, a small metal nanoparticle accelerates the decomposition of a silicon-containing gas; the silicon atoms precipitate at the interface between the nanoparticle and the substrate, forming a column of silicon (i.e. a nanowire) with the desired high surface-to-volume ratio, as shown in Fig. 1.

To obtain a dense array of nanowires between two electrodes, we first form the electrodes and then grow the nanowires from one electrode toward the other. To form a suitable electrode structure from which nanowires can grow, we use previous observations that nanowires grow preferentially perpendicular to (111) surfaces [5, 13]. When the (111) planes are oriented vertically, the nanowires grow laterally, as we desire in our application. To form electrodes with parallel, vertical (111) surfaces, we use the well-known technique of anisotropic, wet chemical etching of a (110)-oriented Si wafer [28]. This orientation of Si has two sets of (111) planes perpendicular to the surface. Because the features being defined by etching are the electrodes connecting the nanowires to the microscale electronics, they can be patterned by conventional lithography. After the electrodes are defined, a very thin layer of catalyst is deposited on the walls of the electrodes and annealed to form isolated nanoparticles of the catalyst material. The structure is then exposed to a silicon-containing precursor gas in a chemical vapor deposition (CVD) reactor. The decomposition of the gas is slow on bare silicon surfaces, but is greatly accelerated at a catalyst nanoparticle. The resulting silicon atoms diffuse through or around the catalyst nanoparticle and precipitate at the nanoparticle–substrate interface, pushing the nanoparticle away from the surface. The column of silicon left behind is the desired nanowire.

The nanowire grows across the trench toward the (111)-oriented side wall of the opposing electrode. When the nanowire reaches the opposite side wall, it touches and then is 'welded' to the side wall by continued catalyzed decomposition, as will be described later. The connection is found to be mechanically strong. If the surface of the nanowire is properly treated, the conductance of the nanowire and the current flowing between the two electrodes can be modulated by a nearby charged species. Because of its high surface-to-volume ratio and small diameter, the nanowire can serve as an efficient chemical or gas sensor. By using a large number of such 'nanobridges' in parallel, the desired high surface area can be obtained in a small overall volume.

3 Experimental demonstration of the bridging technique

As reported previously [6], to demonstrate the concept we formed a trench bounded by vertical surfaces in a (110)-oriented silicon wafer using conventional, coarse lithography (Fig. 2a and c). First, the wafer was covered with an etch-resistant layer of thermally grown silicon dioxide, and reactive ion etching with CHF_3 and Ar gases was used to form an opening in the oxide layer. The silicon was then etched through this opening using an aqueous solution containing KOH (44% KOH–H_2O at 110 °C for 1 min), which etches different crystal orientations of silicon at different rates. With (110)-oriented silicon and a masking layer with its edges aligned perpendicular to ⟨111⟩ directions of the substrate, the vertical etching rate is much greater than the lateral etching rate (by as much as 100:1) [28], leaving vertical, (111)-oriented silicon surfaces bounding the trench. In this work, the trenches are approximately 8-μm deep and 2–15-μm wide.

After forming the vertical (111) surfaces, the nucleating metal catalyst – titanium or gold on the order of 1 nm average thickness – was deposited by electron-beam evaporation onto the vertical surfaces of the etched grooves as shown in Fig. 2b. Titanium is especially attractive because of its compatibility with silicon technology [5]. In the present demonstration, the catalyst was deposited only on one side wall of the trench by angled evaporation so that the initiating and impinging ends of the nanowires could be studied separately. Because of the geometry of the structure and deposition angle, no catalyst was deposited on the bottoms of trenches narrower than 8 μm. After inserting the samples into the chemical vapor deposition reactor, they were annealed in hydrogen to form Au–Si alloy nanoparticles or to reduce the native oxide on Ti and form

FIGURE 1 Schematic illustration of metal-catalyzed nanowire growth using chemical vapor deposition. A small metal nanoparticle accelerates the decomposition of a silicon-containing gas; the silicon atoms precipitate between the nanoparticle and the substrate, forming a column of silicon

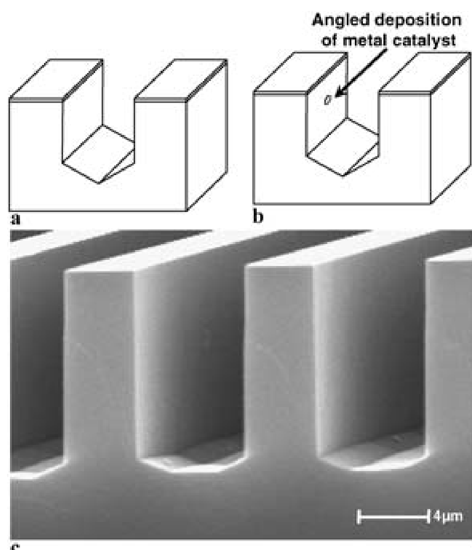

FIGURE 2 **a** Schematic and **c** scanning electron micrograph of 6-μm-wide trench formed in (110)-oriented silicon. Some ledges are visible on the side walls. **b** Schematic showing catalyst deposited on vertical side wall of trench

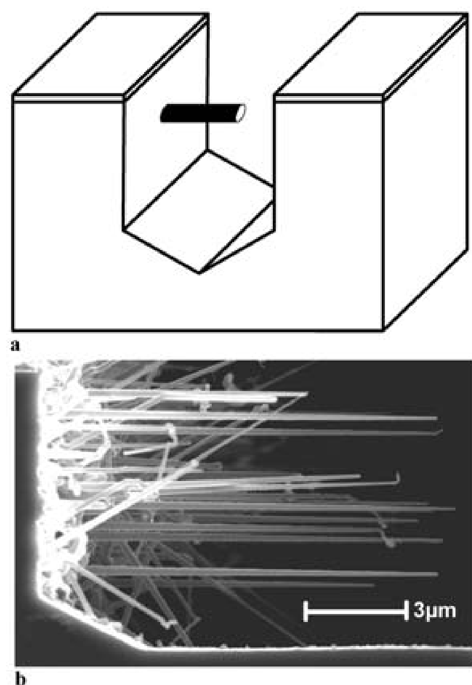

FIGURE 3 **a** Schematic view and **b** cross-section scanning electron micrograph of lateral epitaxial nanowire growth from (111)-oriented side wall surface plane at the *left* of the diagrams into a 15-μm-wide trench

$TiSi_2$. A mixture of SiH_4 and HCl was then introduced into the hydrogen ambient to grow the nanowires at $\sim 640\,°C$.

Using this technique, we demonstrated lateral growth and mechanical connection of nanowires across the trench using both Ti and Au catalysts [6]. Figure 3 illustrates Au-nucleated Si nanowires growing laterally from one (111)-oriented trench face toward the opposing face and extending partially across a 15-μm-wide trench. For gaps 8-μm wide or less, many Au-nucleated nanowires extend completely across the trench, as shown for an 8-μm-wide trench in Fig. 4. Approximately 70% of them intersect the opposing side wall at an angle of $90° \pm 0.5°$.

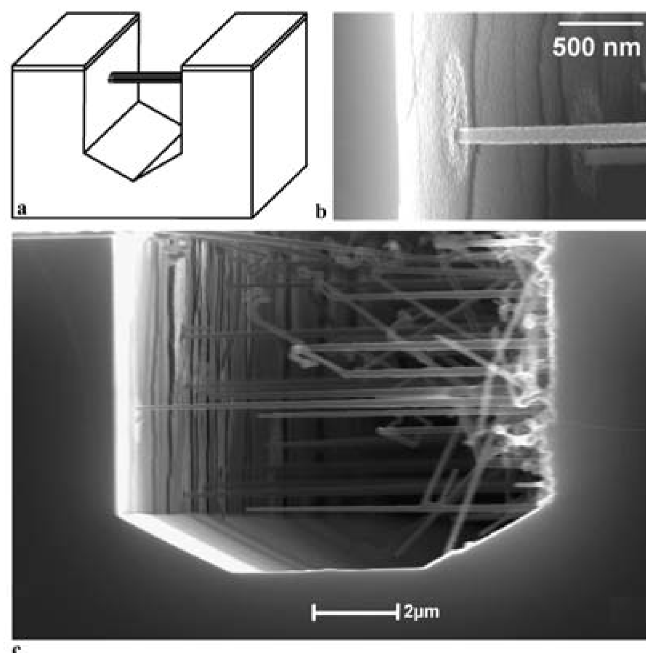

FIGURE 4 **a** Schematic and **c** scanning electron micrograph of nanowires ‘bridging’ across 8-μm-wide trench and connecting to opposing side wall. The nanowires grow from *right* to *left* in these views. **b** Impinging-end disk, showing the details of connection

3.1 *Mechanical and structural characteristics of the bridging nanowires*

To use these nanowires as sensors, the connection between the side wall and the impinging nanowire must be mechanically strong. In the case of Au-nucleated Si nanowires, the catalyzing nanoparticle at the tip of the growing nanowire is in the liquid state during nanowire growth. After impinging, the catalyst and, therefore, the accelerated Si growth spread along the side wall a controllable distance, firmly connecting the nanowire to the side wall. In the case

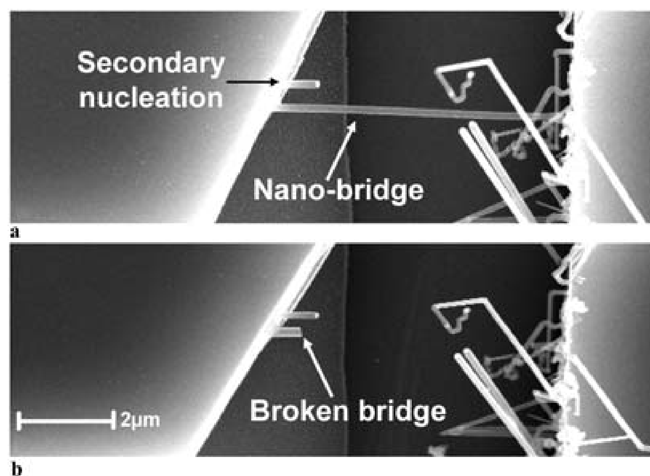

FIGURE 5 Structural and mechanical robustness of the nanobridges. **a** A single nanowire bridging between electrodes. **b** The same region after manually breaking the nanowire (*arrow*) using a tungsten probe. The nanowire broke along its length, rather than at the connection point, demonstrating the strength of the connection

of Ti-nucleated nanowires, the catalyzing nanoparticle is in the solid state during growth, so growth along the side wall does not extend as far, but it is sufficient to firmly attach the nanowire to the side wall. The strength of the connection is indicated by the nanowires often breaking along their length, rather than at the connection point, when they are stressed to failure. Figure 5 shows a single nanowire bridge that was manually broken by applying pressure using a tungsten probe. The impinging end of the broken nanowire is still attached to the side-wall electrode, demonstrating the mechanical strength of the connection.

To further investigate the connection between the impinging end of the nanowire and the side wall, we treated a sample containing gold-catalyzed nanowires grown across a trench in a 1:1 hydrofluoric acid HF : H_2O solution for ~ 100 min. (This concentration of HF is greater than that conventionally used in IC processing.) Even after this extended exposure to the high-concentration HF solution, the nanowires remain attached to the side walls. The Au–Si alloy layer has been partially removed from the side wall of the grooves, but the Si nanowires are still attached to the side walls, suggesting Si–Si bonding. Although the diameters of the nanowires are generally unchanged by this HF treatment, the nanowire surfaces become rough and the diameter near the tips is slightly reduced [29].

As nanowires grow across trenches between electrodes, they are unsupported and are subject to forces of gravity, of the gas flow in the reactor, and of mechanical vibrations created by pumps and cooling fans. (Although the forces from gas flow would be large in the forced-convection region of the deposition chamber, they are expected to be significantly lower in the boundary layer near the substrate surface.) During growth the nanowires are supported at only one end until bridging occurs; after that, the nanowires are supported at both ends for device applications. During use, the nanowires are subject to forces from mechanical motion of the entire device structure. When used as sensors, the motion of nearby fluid can also place stress on the nanowires. Because semiconductors are generally stiff and brittle materials, these mechanical forces must be considered when designing lateral nanowire bridges to ensure their mechanical robustness both during growth and during use.

We carried out theoretical calculations to qualitatively correlate the strength of a bridged nanowire with its length and diameter. In our simulations, a nanowire is approximated as a solid beam (with circular cross section) made of single-crystal Si and is connected to two vertical Si walls. The root and the tip of the nanowire are connected to the walls with defect-free, single-crystal bonding with no variations of the crystal properties at the interface. To obtain an indication of the trends affecting the strength of a nanowire, the standard relationships between tensile stress, stiffness (168 GPa), and strain are used to find the maximum length of a nanowire that is able to resist plastic deformation or fracture due to gravitational forces [30]. This calculation shows that a nanowire with 10-nm diameter will collapse due to its own weight if the length exceeds $\sim 40\,\mu$m, while a nanowire with 100-nm diameter can be up to ~ 800-μm long before failure. These numbers should only be used for a qualitative understanding of the mechanical limits of a bridged-nanowire device; other factors, such as stress caused by native oxide, must also be considered. In applications such as sensors, nanowires will also be subject to fluidic pressure from the flowing gas or liquid being sensed. In addition to the strength of the nanowire itself, the strength of the connection between the nanowire and the electrode is crucial to ensure high device reliability.

For a (110)-oriented Si wafer, the etching depends sensitively on the in-plane crystallographic orientation of the mask edge defining the region to be etched, and accurately orienting the mask with the substrate is critical. For example, severe undercutting of the mask occurs without accurate orientation. Mask misorientation also leads to ledges in the vertical side walls of the grooves. The ledges contain many steps and kinks, which can extend from the top of the trench to the bottom. Although normally undesirable, these irregularities may offer some advantages for preferentially positioning the

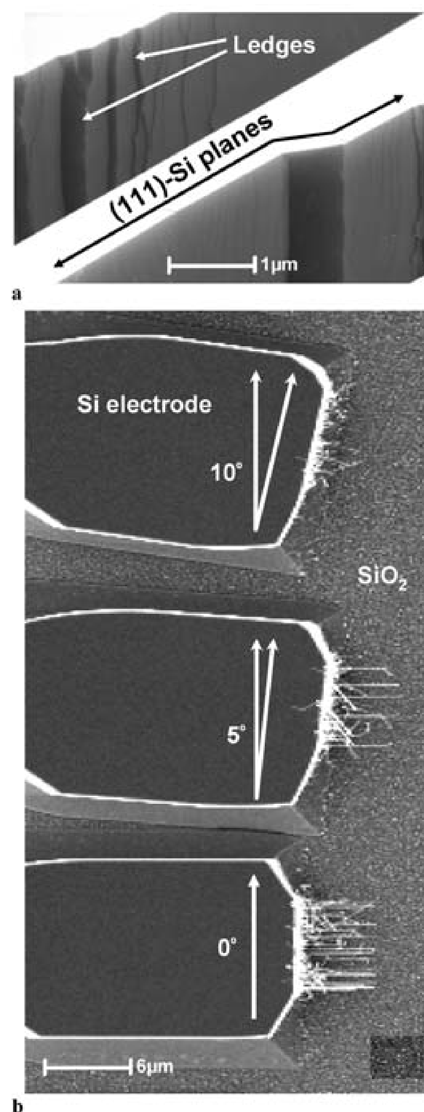

FIGURE 6 **a** Ledges on the side walls of electrodes due to mask misorientation by $\sim 10°$ with respect to the (111) planes. **b** Three electrodes with 0, 5, and 10° misorientation. Very few nanowires grow on the electrode with 10° misorientation while the nanowire density is highest (~ 15) for the well-aligned electrode. For 5° misorientation, more than half of the nanowires are misoriented; only six nanowires grow in the expected direction

catalyst nanoparticles; the higher density of broken bonds in these regions may create low-energy sites for catalytic nuclei. Figure 6a shows ledges on the side walls of electrodes due to a mask misorientation by $\sim 10°$. The density and orientation of grown nanowires vary because of different ledge densities on misoriented electrodes. Figure 6b illustrates three electrodes with 0, 5, and 10° misorientation. The density of (111)-oriented nanowires is very low for the electrode with 10° misorientation, while it is highest for the well-aligned electrode. Although the same amount of metal catalyst was deposited on the side walls, the number of nanowires diminished markedly to a few nanowires for the misoriented electrodes. Understanding the correlation between the degree of misorientation and the density of nanowires will be useful.

In addition to primary nanowire growth from the deposited catalyst, nanowires were also nucleated from the catalyst transported across the trench at the tip of the growing nanowires. Such secondary nucleation was observed on the (111) plane at the impinging end of a nanowire for both Au and Ti catalysts; tertiary nucleation was observed with Au catalyst. A majority of the nanowires formed by secondary nucleation are perpendicular to the (111) surface and grow in close proximity to the corresponding primary nanowires, as shown in Fig. 7a. A small fraction of the nanowires formed by secondary and tertiary nucleation grow along other (111) directions, which make an angle of $\sim 70°$ with the primary nanowire as illustrated in Fig. 7b and c. Higher-order nucleation may find application in nanophotonics and nanoelectronics.

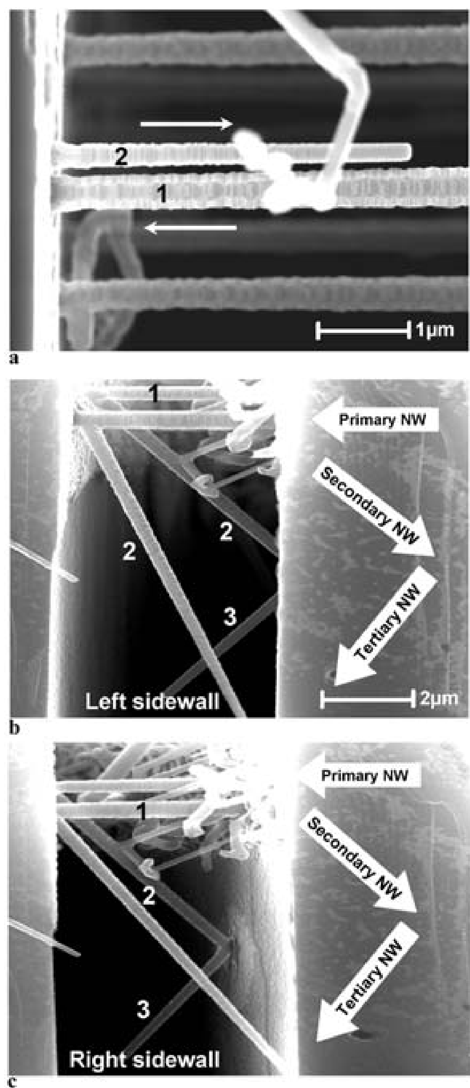

FIGURE 7 **a** Secondary nanowire (labeled 2) grown from the disk formed at the impinging end of a gold-nucleated, bridging Si nanowire. **b** and **c** Secondary nanowires (labeled 2) and tertiary nanowires (labeled 3) grown at an angle of 70° with the primary nanowire

4 Nanobridges with electrically isolated electrodes

To form functioning nanodevices, the electrodes must be isolated from each other, from electrodes of other devices, and from the substrate, which might contain other electronic components. Electrical isolation can be provided by forming the electrodes from a heavily doped, (110)-oriented, top silicon layer of a silicon-on-insulator (SOI) structure, in which a layer of silicon dioxide separates the top silicon layer from the mechanically supporting underlying silicon wafer, as schematically illustrated in Fig. 8a. Removing the entire thickness of the top silicon layer between the electrodes provides the necessary electrical isolation (Fig. 8b). Because the two sets of (111) planes perpendicular to the surface of a (110)-oriented layer are oriented at 70° to each other, patterns with 70° corners produce the best-defined electrodes. The corners also etch crystallographically, leading to enhanced undercutting at the corners. Properly defining the electrode features on the mask can minimize this undercutting [31]. Measurements of current–voltage characteristics between isolated electrodes spaced 10-µm apart and separated from the substrate by a 120-nm-thick oxide layer show a leakage current of only a few picoamperes with 5 V applied.

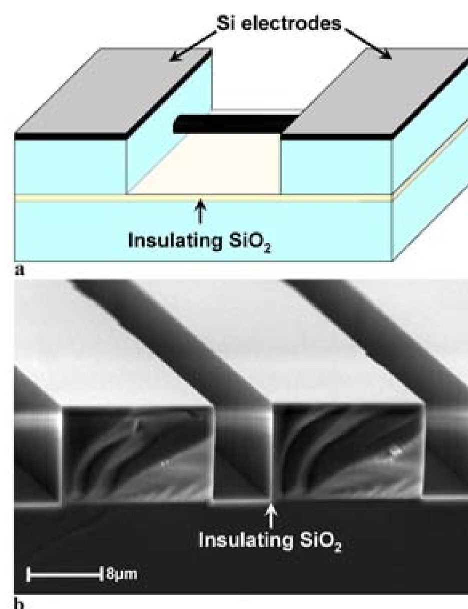

FIGURE 8 **a** Schematic diagram of bridging nanowire on an SOI substrate, which provides electrical isolation. **b** Scanning electron micrograph of SOI substrate after the formation of electrodes with vertical side walls

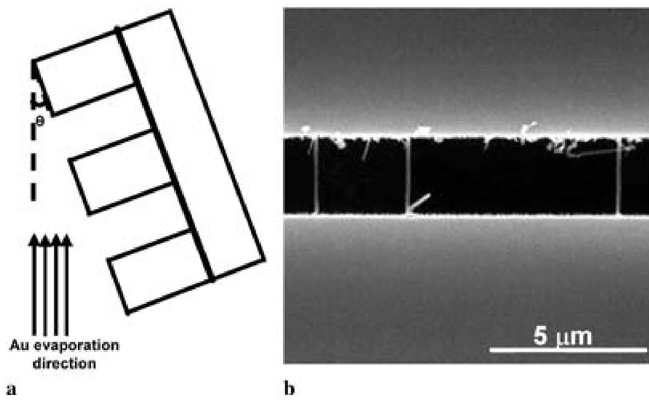

FIGURE 9 **a** Schematic diagram of angled metal evaporation. **b** Plan-view scanning electron micrograph, showing selective growth of nanowires from the vertical side walls, with no growth on horizontal surfaces

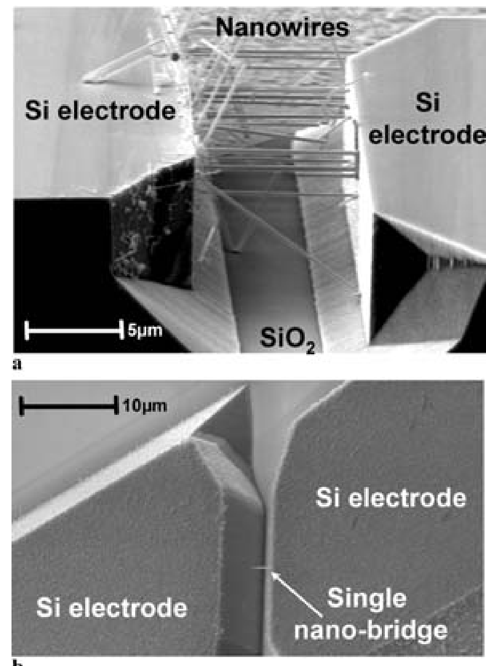

FIGURE 10 Silicon nanowires grown from the vertical side walls of isolated electrodes. The horizontal surfaces are free of nanowires. Uncatalyzed silicon deposition is extremely slow on the electrodes. **a** depicts ∼ 15 nanobridges while **b** shows a single nanobridge

After etching the top masking oxide by conventional reactive-ion etching, the silicon is etched in KOH, as described above, until the underlying oxide layer is exposed. For ease of making subsequent electrical contact, the masking oxide on top of the electrodes can be removed before further processing, but the oxide layer separating the top silicon layer from the substrate must remain to provide the needed electrical isolation.

After defining the electrodes, the catalyst is evaporated at an angle θ ($\theta \neq 90°$) to the substrate surface plane, as shown in Fig. 9a, so that it is deposited on one of the side walls of the trenches between the electrodes. Nanowire growth depends on the size of the catalyzing nanoparticles at the start of the deposition process, and consequently on the amount of catalyst deposited on the surface and the subsequent thermal treatments. In the case of gold, if the amount of gold deposited on the exposed silicon surface is less than a critical amount, the nanoparticles are too small to enable nanowire growth. The dependence on the amount of gold deposited can be used to selectively form nanowires on some surfaces without growing them on other surfaces, thus simplifying further processing. If gold is evaporated at a small angle θ from the surface plane of the wafer, the thickness of gold deposited on the vertical surfaces is $d \cos\theta$, where d is the thickness if the substrate surface is held normal to the beam of evaporated material. The thickness of gold deposited on horizontal surfaces is $d \sin\theta$. If θ is chosen to be small (e.g. $\sim 20°$), the amount of catalyst on vertical surfaces is above the critical thickness for nanowire growth, while that on horizontal surfaces is below the critical thickness. Therefore, nanowires grow from the vertical surfaces, as desired, while none grow on horizontal surfaces, as shown in Fig. 9b, simplifying subsequent processing. Figure 10a shows two isolated electrodes bridged by ~ 15 nanowires, while Fig. 10b shows electrodes bridged by a single nanowire.

In addition to avoiding nanowire growth on the silicon at the top of the electrodes, we need to ensure that no catalyst is on the exposed oxide layer between the electrodes. Because of the shadowing of the bottom oxide by the electrode, catalyst deposition can readily be avoided between electrodes. Adjacent to the electrodes, however, the oxide surface is exposed to the incoming beam of catalyst atoms. The catalyst deposited on the oxide accelerates decomposition of SiH_4, leading to spurious deposition on the oxide adjacent to the electrodes and providing a path for leakage current between the electrodes. Therefore, deposition of the catalyst on the exposed oxide must be avoided, or the catalyst must be selectively removed from these regions before nanowire growth. Because of the different amounts of catalyst deposited on horizontal and vertical surfaces and the different behavior on silicon and on oxide during annealing, the catalyst can be removed selectively by careful and optimized etching.

4.1 *Doping of nanowires*

For use in an electronic device, adding dopants to the nanowires may be necessary. For thicker, gold-catalyzed nanowires, we have been able to incorporate boron into the nanowires during growth by adding the p-type dopant diborane (B_2H_6) to the $H_2/SiH_4/HCl$ ambient in the deposition chamber. Current–voltage measurements between two electrodes indicate that the boron-dopant concentration increases with increasing B_2H_6 partial pressure in the deposition ambient. These electrical measurements and the dimensions of the nanowires indicate that boron concentrations in the low-$10^{18}\,cm^{-3}$ range were incorporated into the nanowires. This concentration is of the same magnitude as that found for epitaxial silicon deposition on a plane silicon surface, indicating that doping thicker nanowires is feasible and that the current is not limited by contact resistance between the p-type nanowires and the p-type electrodes. The current–voltage characteristic is linear, again suggesting that the nanowires make good electrical contact to the electrodes during growth. Figure 11 shows the linear current–voltage characteristic between an electrode pair connected by six bridging nanowires.

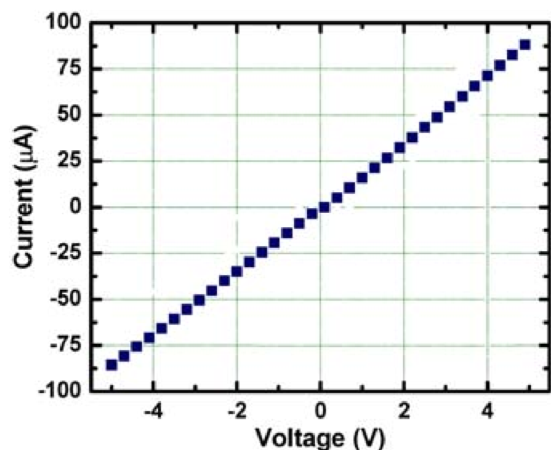

FIGURE 11 Measured I–V characteristics between bridged electrodes spaced 10-μm apart and joined by six nanowires. The average resistance of a nanowire is measured to be 350 kΩ

Doping thinner nanowires is expected to be more complex because of the closer proximity to the surface and the statistically small number of dopant atoms that would be incorporated into a nanowire a few nanometers in diameter. The dopant atoms might segregate to the surface of the nanowire, or the number of dopant atoms might be so small that a fluctuating potential might impede current flow. Omitting the dopant atoms during growth and adding dopant (if needed) from the surface after growth might provide more robust process control.

For either sensor or field-effect-transistor applications, the conductance of the nanowires must be modulated effectively. When used as a depletion-mode FET, the entire cross section of the nanowire must be depleted. When used as a sensor, the sensitivity can be increased if the conducting region is narrow. Therefore, the maximum thickness of the depletion region can limit the range of useful combinations of doping and diameter. Because the amount of charge that must be depleted to extend the depletion region further decreases as the depletion region extends into the nanowire, the maximum depletion-region thickness is greater for a nanowire than for a plane surface. From a one-dimensional analysis in radial coordinates using the complete-depletion approximation, the maximum thickness of the depletion region is given by the common formula for $x_{d\max}$ of a plane structure multiplied by a factor of $\sqrt{3}$. For a nanowire diameter of 20 nm, the maximum dopant concentration that allows complete depletion is in the mid-10^{19} cm^{-3} range. For somewhat thinner nanowires, the maximum dopant concentration is limited by the solid solubility of the dopant in Si. For narrow nanowires, quantum effects may also modify the electrical behavior.

5 Conclusion

We have demonstrated the growth of laterally oriented, metal-catalyzed Si nanowires bridging between vertical (111) Si planes formed by anisotropically etching a (110)-oriented SOI wafer. These electrically connected and mechanically robust nanobridges resist considerable force. They can be made electrically conducting by adding dopant atoms during nanowire growth, and the conduction is not limited by contact resistance in the doping range investigated. By employing only optical lithography in addition to nanowire growth, a large array of nanoscale sensors can be fabricated between biasing electrodes. This nanowire structure combines the advantages of ‘bottom-up’ fabrication of nanostructures with ‘top-down’ formation of the connecting electrodes using only coarse optical lithography. It offers the possibility of fabricating nanoscale electronic devices without costly and slow fine-scale lithography. Nanobridges constructed by the method described here may be capable of integration with more conventional electronics to provide additional functionality. This enhanced functionality may be especially valuable as sensing and computation become distributed throughout the environment.

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